SimuLED

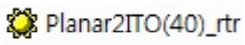
LED epi-chip Simulation Software
(SiLENSe/SpeCLED/RATRO)

SimuLED 구성

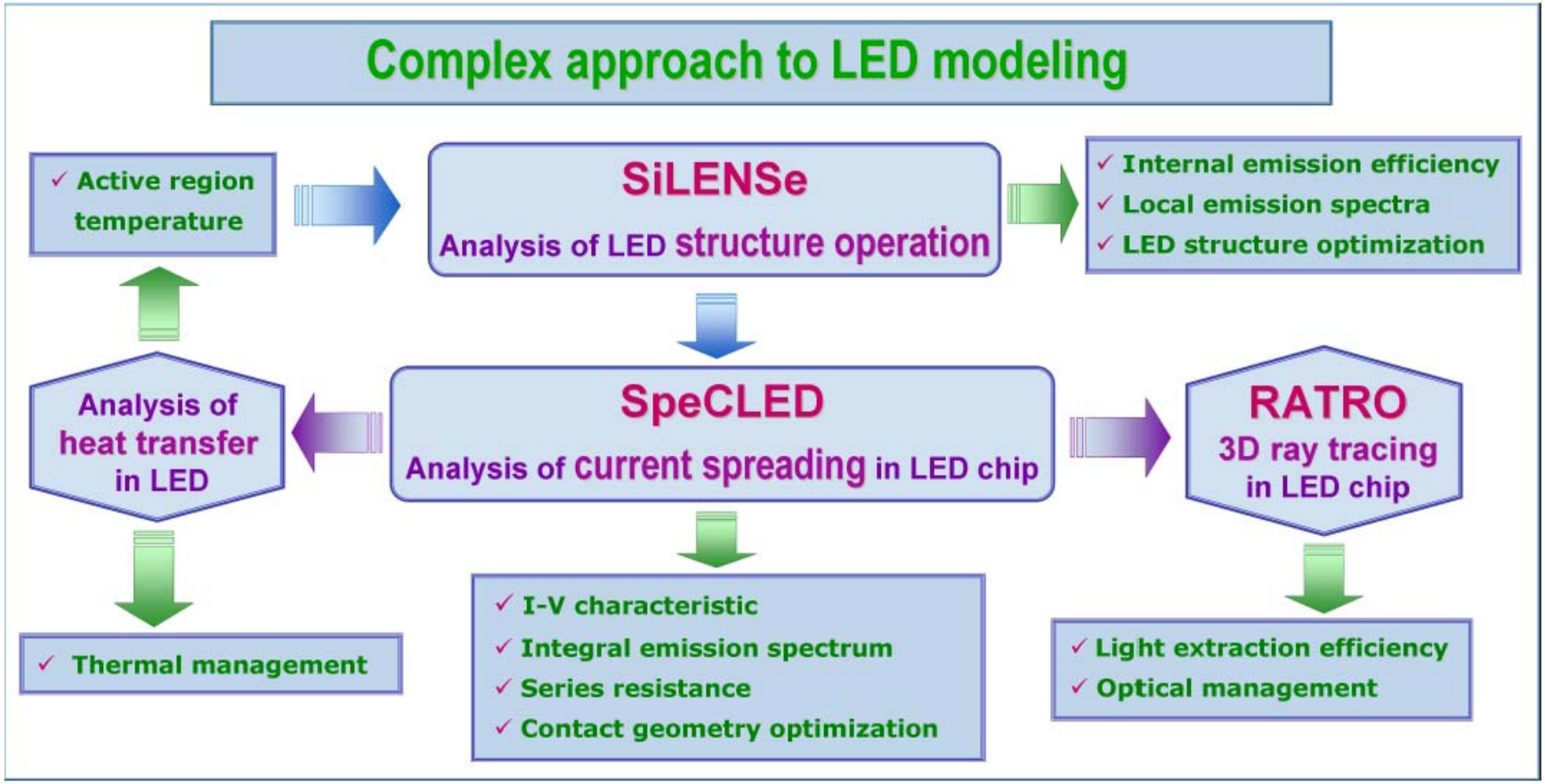
- **1. SiLENSe**(LED heterostructure 최적화)
  -Material properties editor (SiLENSe 기본 물성 편집)
  -project input file(".sls"), output file(".sls")

- **2. SpeCLED**(ITO,BL,electrode 구조 최적화)
  -project input file(".dvx"), output file("~_(40).cgs")
  ~_(40).cgs: 칩에 40mA 전류가 흐를 때 결과값

- **3. RATRO**(Chip level 광추출 효율/ 광분포 최적화)
  -project input file(".dvx"). Output file("(40)_rtr.cgs")



SimuLED 개념도


Complex approach to LED modeling
✓ Active region temperature
SiLENSe
Analysis of LED structure operation
✓ Internal emission efficiency
✓ Local emission spectra
✓ LED structure optimization
Analysis of heat transfer in LED
SpeCLED
Analysis of current spreading in LED chip
RATRO
3D ray tracing in LED chip
✓ Thermal management
✓ I-V characteristic
✓ Integral emission spectrum
✓ Series resistance
✓ Contact geometry optimization
✓ Light extraction efficiency
✓ Optical management

1. SiLENSe

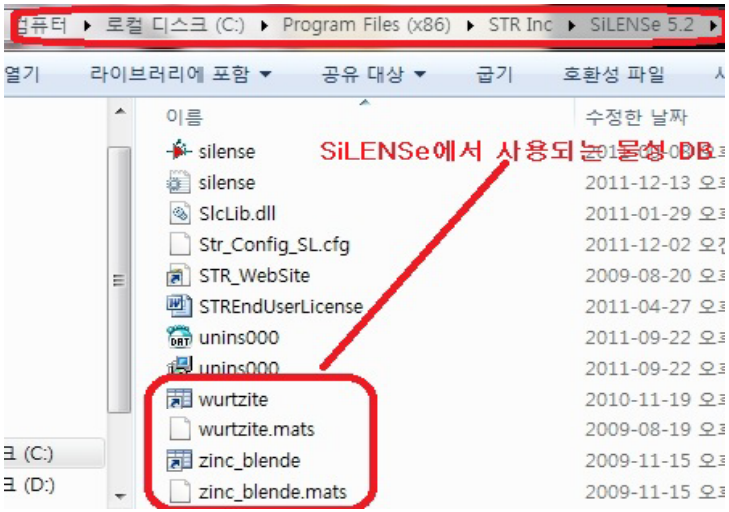
- 0. Material Properties(ProEdit)
  -SiLENSe에서 사용되는 물성 정보의 확인 및 편집기
  -SiLENSe 시작하기 전 Default parameter 물성 확인

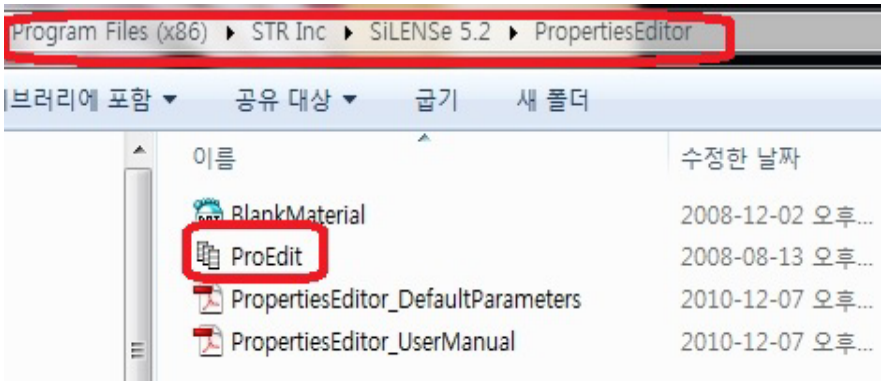
- 1. Input parameters
  - 1-1 degree of relaxation
  - 1-2 layer profile
  - 1-3 global parameter

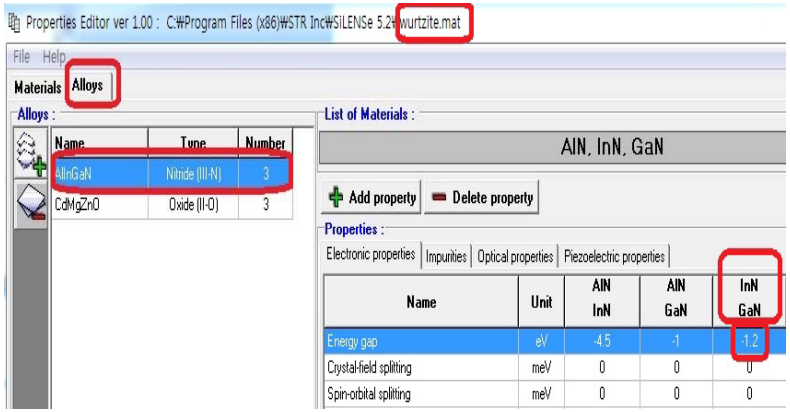
- 2. Output results
  - 2-1 current band diagram
  - 2-2 I-V curve and wavelength

- 3. Export Data into SpeCLED
  - 3-1 to load "J(bias), IQE(J), Spectra(bias)" on the active region of SpeCLED

0. Material properties







1. SiLENSe에서 default로 사용되는 물성 값을 확인/편집 시 필요함
2. InGaN QW이 사용된 LED구조에서 wavelength의 shift가 필요시
   InGaN bowing parameter를 변경할 수 있음, 범위 (-1~-3.4eV, default -1.2eV)

1-1. Degree of relaxation

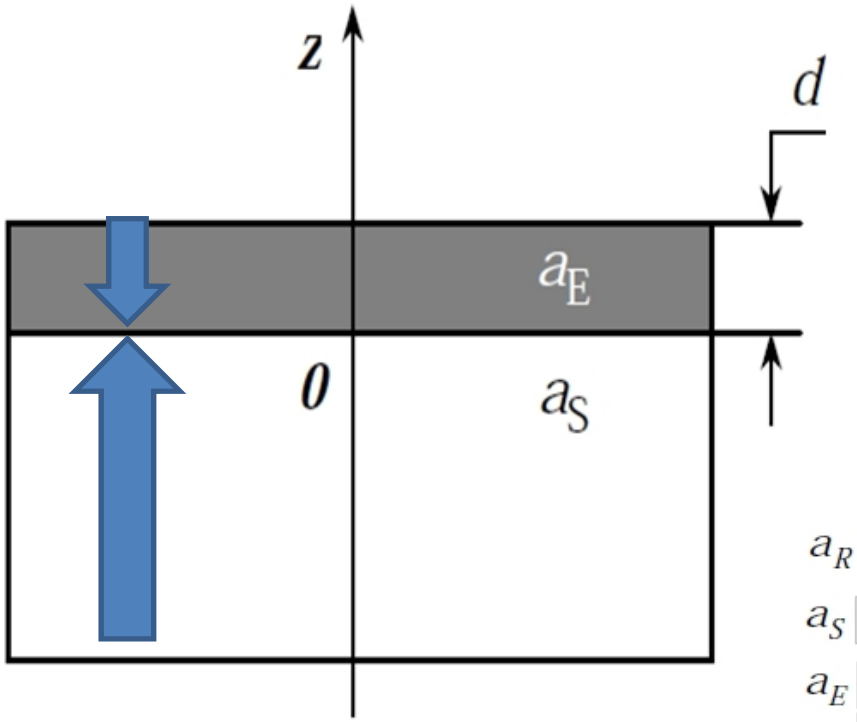


Fig. 1 Epitaxial layer on the underlying layer.

$$a_R(z) = (1-\xi)\cdot a_S + \xi \cdot a_E(z)$$
$$c_R(z) = (1-\xi)\cdot c_S + \xi \cdot c_E(z)$$

degree of relaxation: $0 \le \xi \le 1$

ξ =0, $a_R = a_S$

ξ =1, $a_R = a_E$

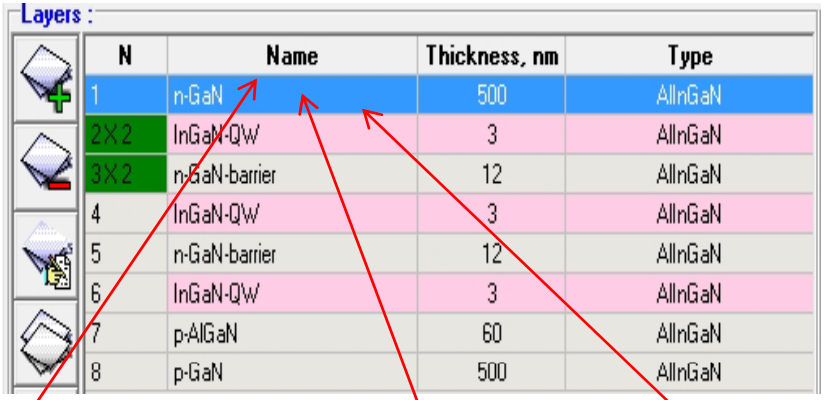
a_R Actual strained lattice constant of the layer

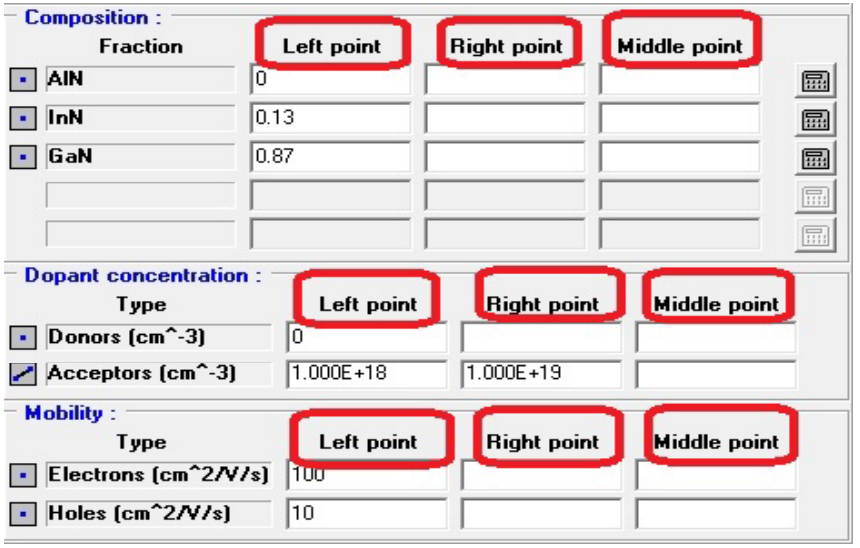
a_S actual lattice constant at the end of the previous layer

a_E in-plane lattice constant of Free-standing layer

[compositon(z), Vegard law(z)]

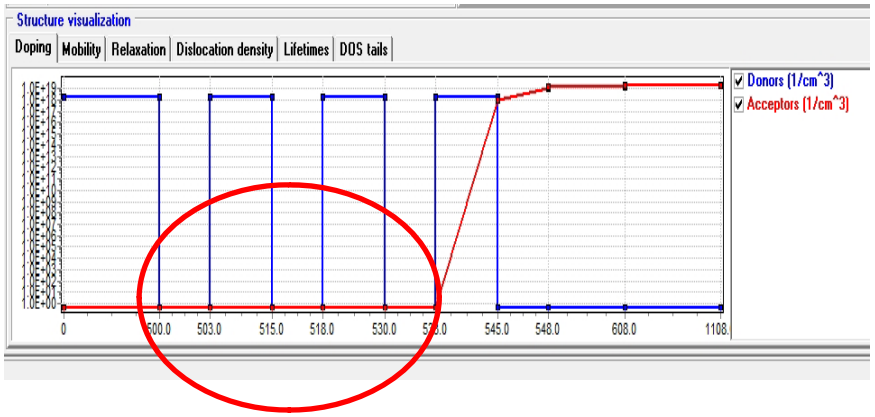
1-2. Layer profile



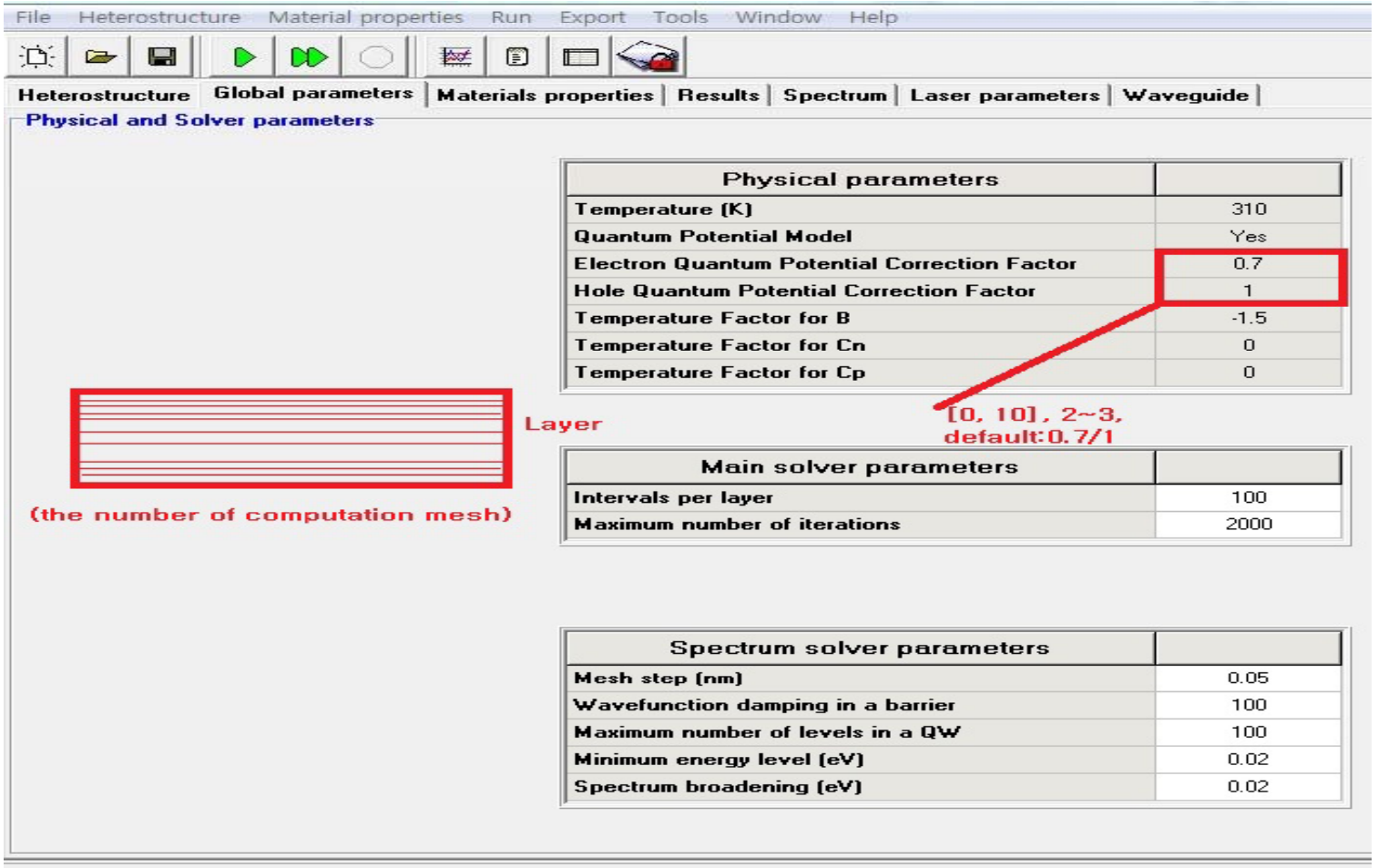


Left(각 layer시점)/middle(각 layer 중점)/right(각 layer끝점)

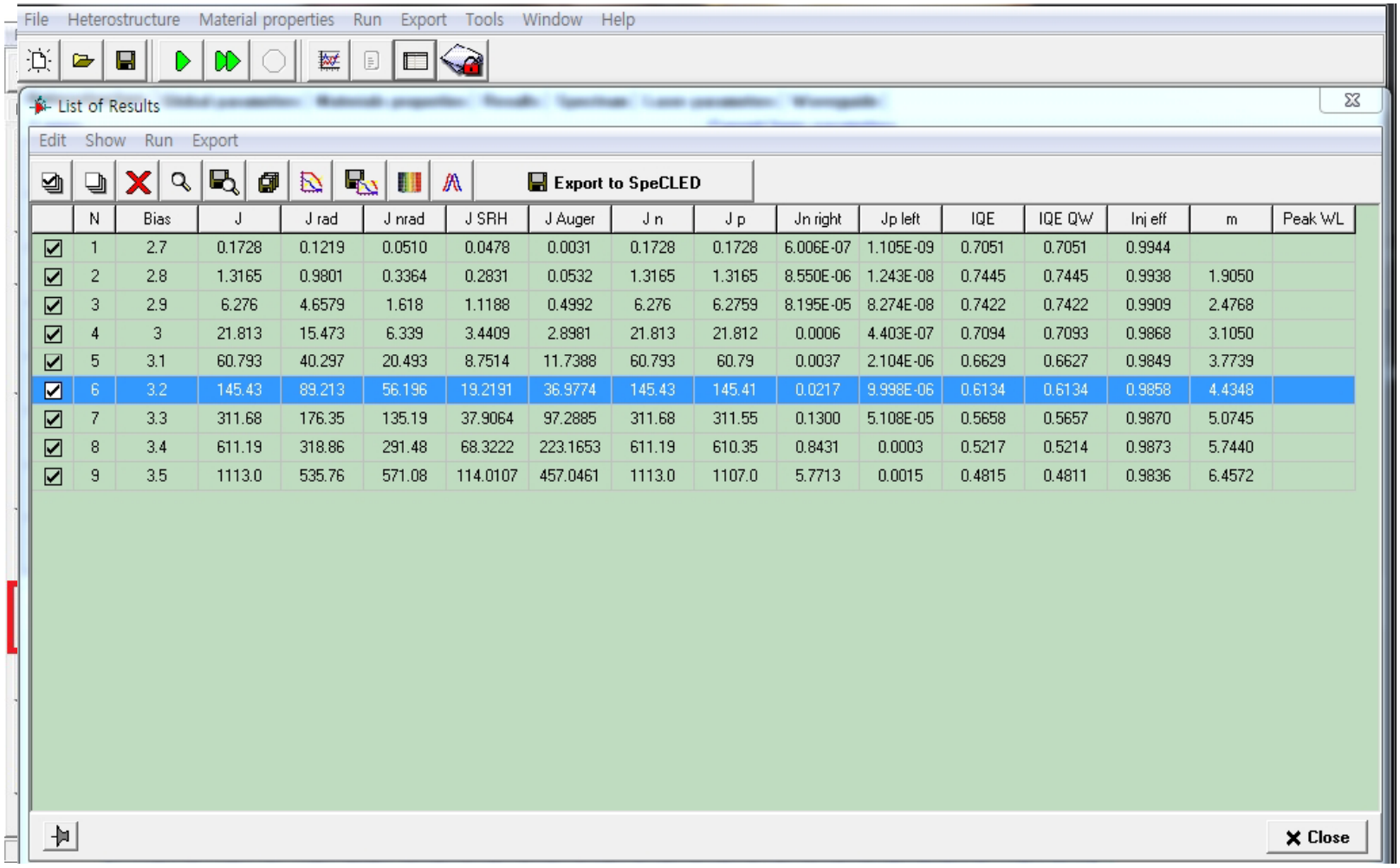
각 layer 물성 정의 시 grade 줄 수 있음
-composition
-dopant
-mobility



1-3. Global parameter

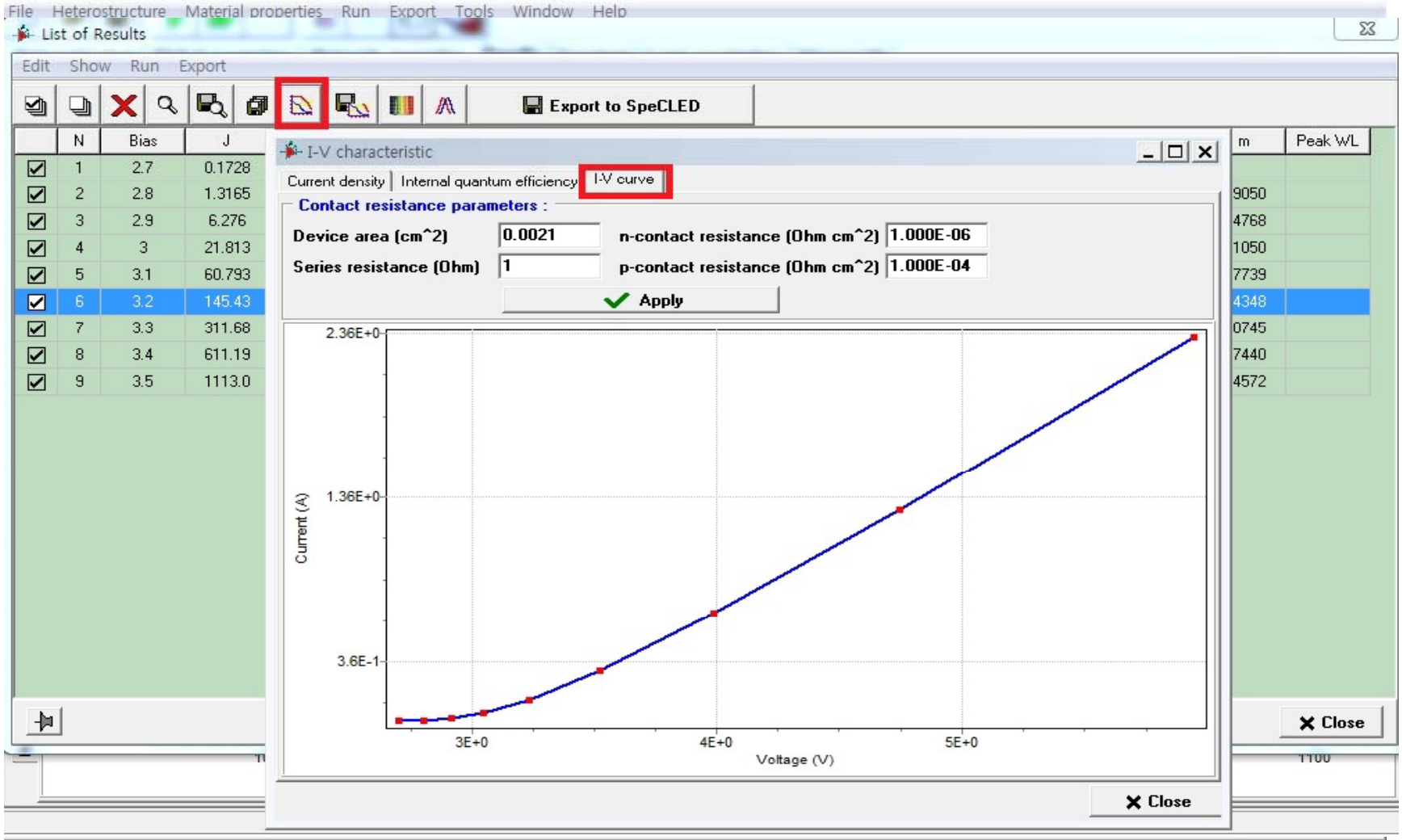


2-1. Current band diagram

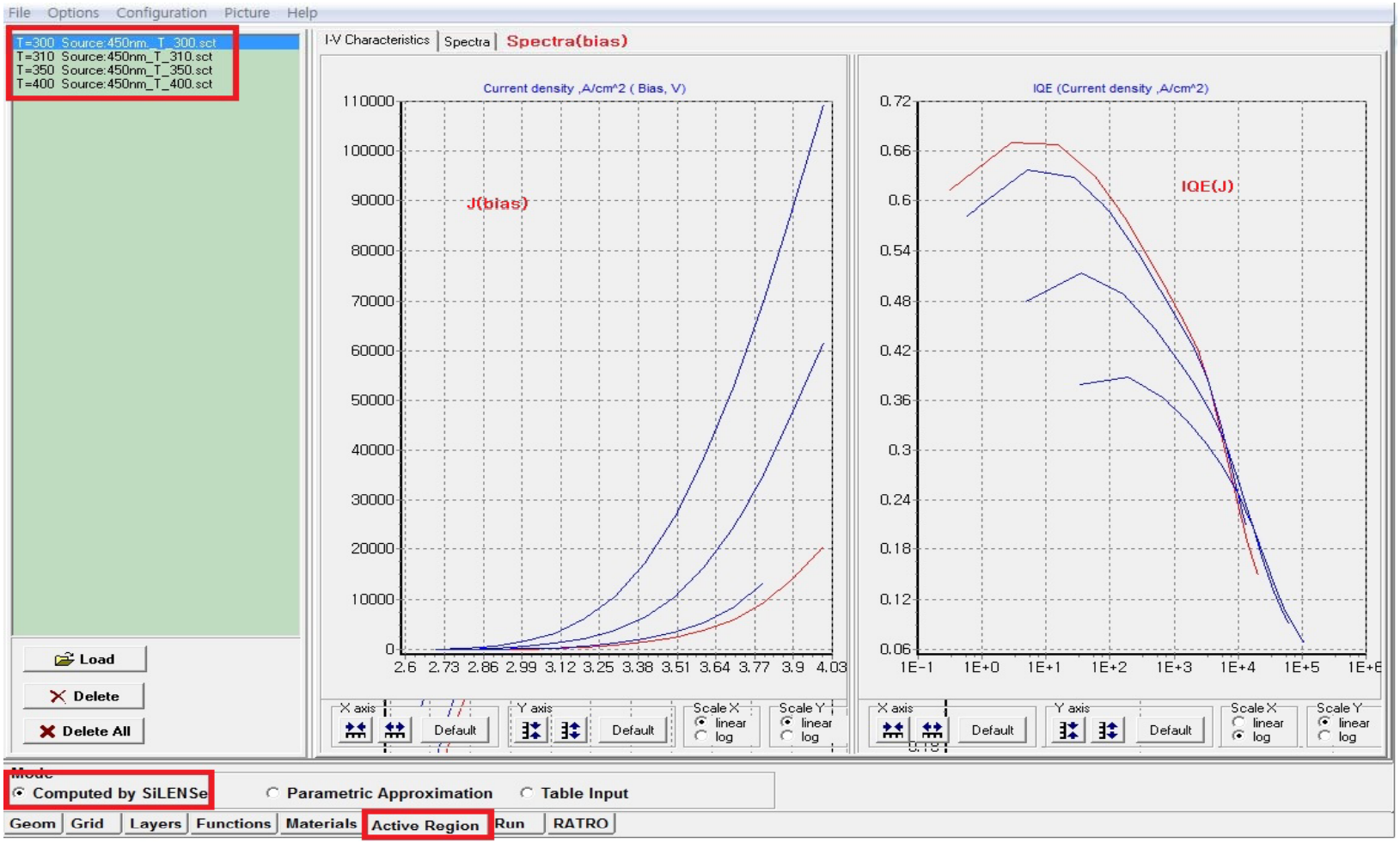


	N	Bias	J	J rad	J nrad	J SRH	J Auger	J n	J p	Jn right	Jp left	IQE	IQE QW	Inj eff	m	Peak WL
☑	1	2.7	0.1728	0.1219	0.0510	0.0478	0.0031	0.1728	0.1728	6.006E-07	1.105E-09	0.7051	0.7051	0.9944		
☑	2	2.8	1.3165	0.9801	0.3364	0.2831	0.0532	1.3165	1.3165	8.550E-06	1.243E-08	0.7445	0.7445	0.9938	1.9050	
☑	3	2.9	6.276	4.6579	1.618	1.1188	0.4992	6.276	6.2759	8.195E-05	8.274E-08	0.7422	0.7422	0.9909	2.4768	
☑	4	3	21.813	15.473	6.339	3.4409	2.8981	21.813	21.812	0.0006	4.403E-07	0.7094	0.7093	0.9868	3.1050	
☑	5	3.1	60.793	40.297	20.493	8.7514	11.7388	60.793	60.79	0.0037	2.104E-06	0.6629	0.6627	0.9849	3.7739	
☑	6	3.2	145.43	89.213	56.196	19.2191	36.9774	145.43	145.41	0.0217	9.998E-06	0.6134	0.6134	0.9858	4.4348	
☑	7	3.3	311.68	176.35	135.19	37.9064	97.2885	311.68	311.55	0.1300	5.108E-05	0.5658	0.5657	0.9870	5.0745	
☑	8	3.4	611.19	318.86	291.48	68.3222	223.1653	611.19	610.35	0.8431	0.0003	0.5217	0.5214	0.9873	5.7440	
☑	9	3.5	1113.0	535.76	571.08	114.0107	457.0461	1113.0	1107.0	5.7713	0.0015	0.4815	0.4811	0.9836	6.4572	

2-2. I-V curve and Wavelength



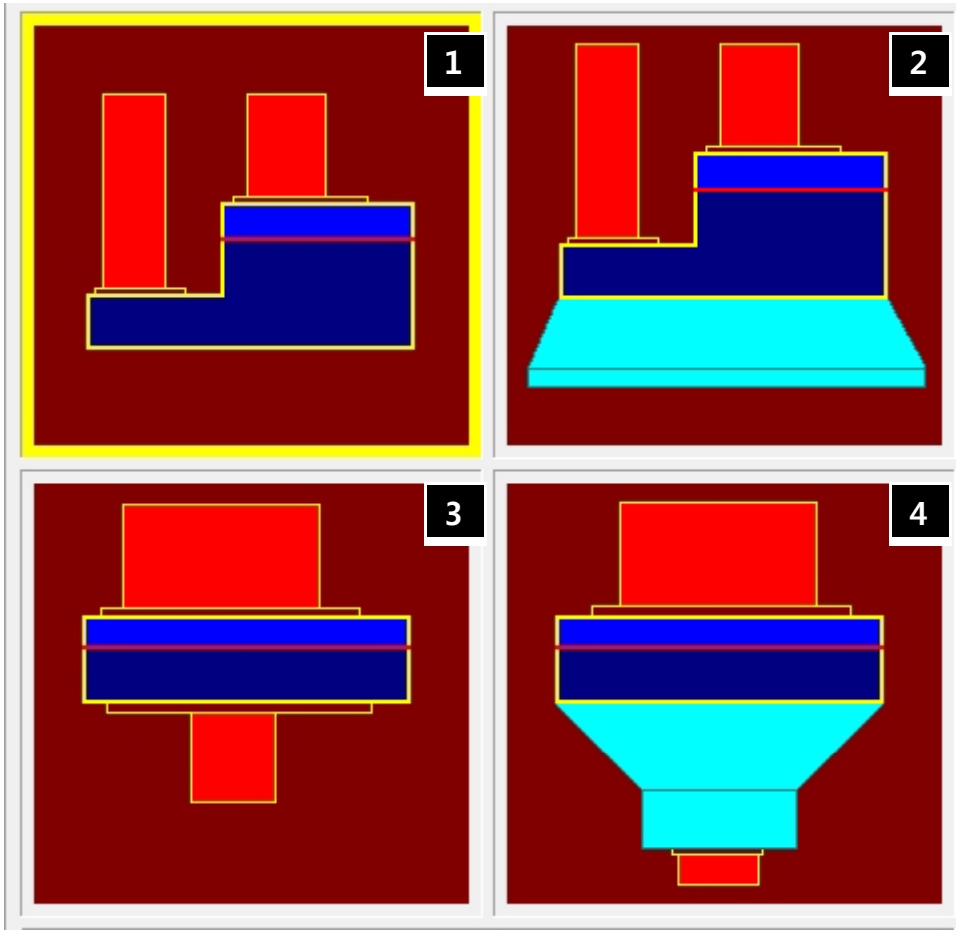
3. Export to SpeCLED



2. SpeCLED

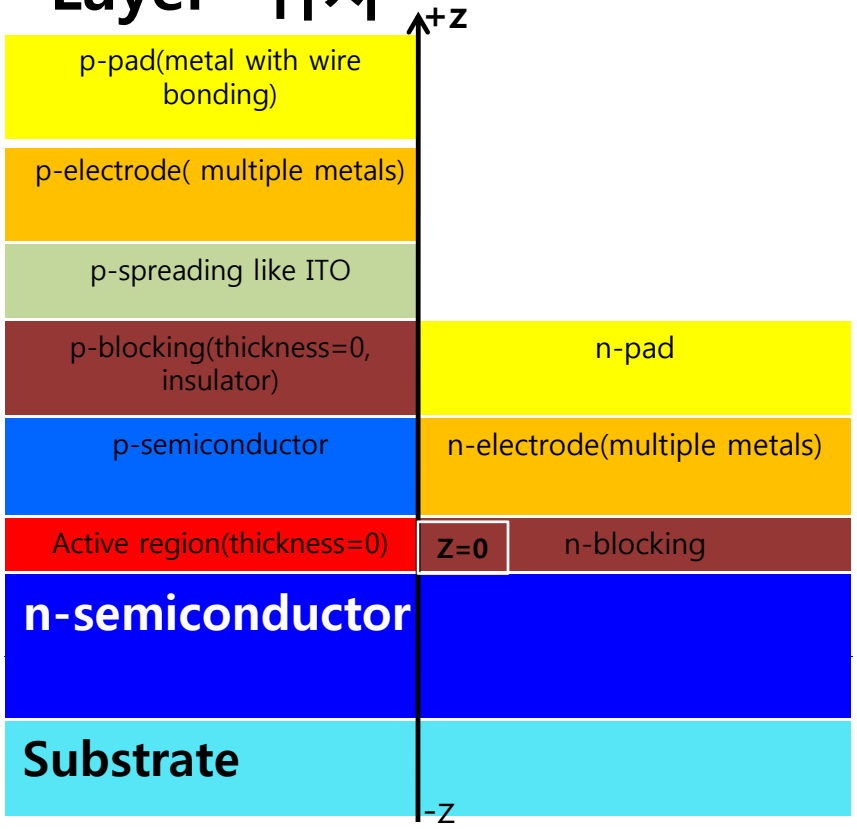
- 2-1. Chip structures available
- 2-2. Layer 위치와 종류
- 2-3. Layer Properties Profile
- 2-4. Computation Vertical mesh
- 2-5. Chip computation mode

2-1. Chip Structures



2-2. layer 위치와 종류

-Layer 위치



-Layer 물성 정의

Layer	물 성
Semiconductor	Mobility,열전도도,전기전도도,도핑 DOS, Ei, g-factor
Conductor	열전도도/ 전기전도도
Spreading	전기전도도 from sheet R
Insulator	열전도도
Substrate	열전도도/전기전도도
Active region(z=0)	J(bias), IQE(J), spectra(bias)

2-3. Layer Properties profile

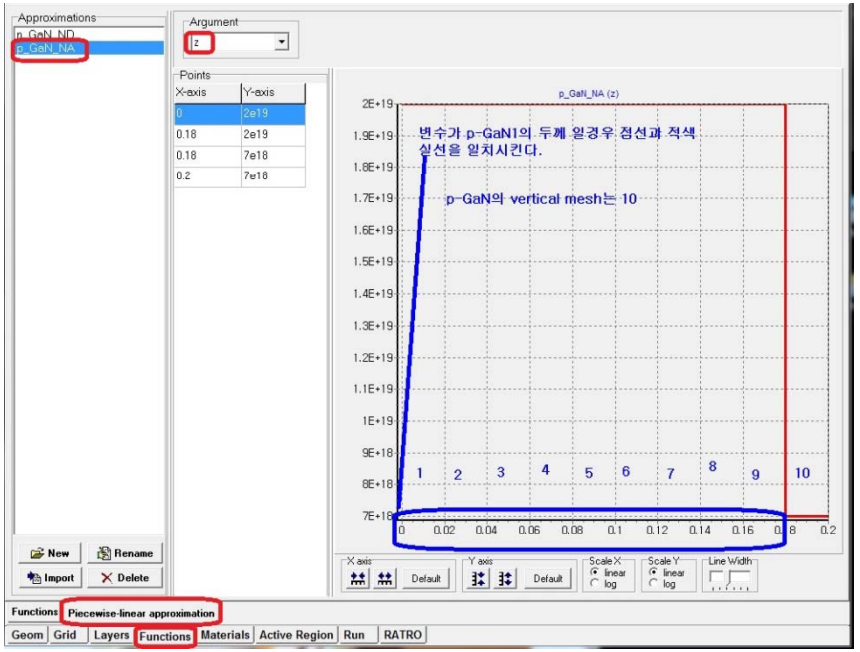
- 2-3-1. p-GaN mobility & doping profile
- 2-3-2. n-GaN mobility & doping profile
- 2-3-3. Vertical mesh
- 2-3-4. Layer contact resistance
- 2-3-5. Heat transfer coefficient

2-3-1. mobility&doping

p-GaN profile

Thickness(+z)	h_Mobility(z,T)	Doping(z)
p-GaN2=0.02um	M=10*(300/T)	5e18
p-GaN1=0.18um	M=8*(300/T)	1e19
z=0		

Piecewise tab in doping(z)



Function tab in mobility(z,T)

```
If (z>0) and (z<0.18) then
    h_mob=8*(300/T);
If (z>0.18um) then
    h_mob=10*(300/T);
Result=h_mob;
```

2-3-2. mobility&doping

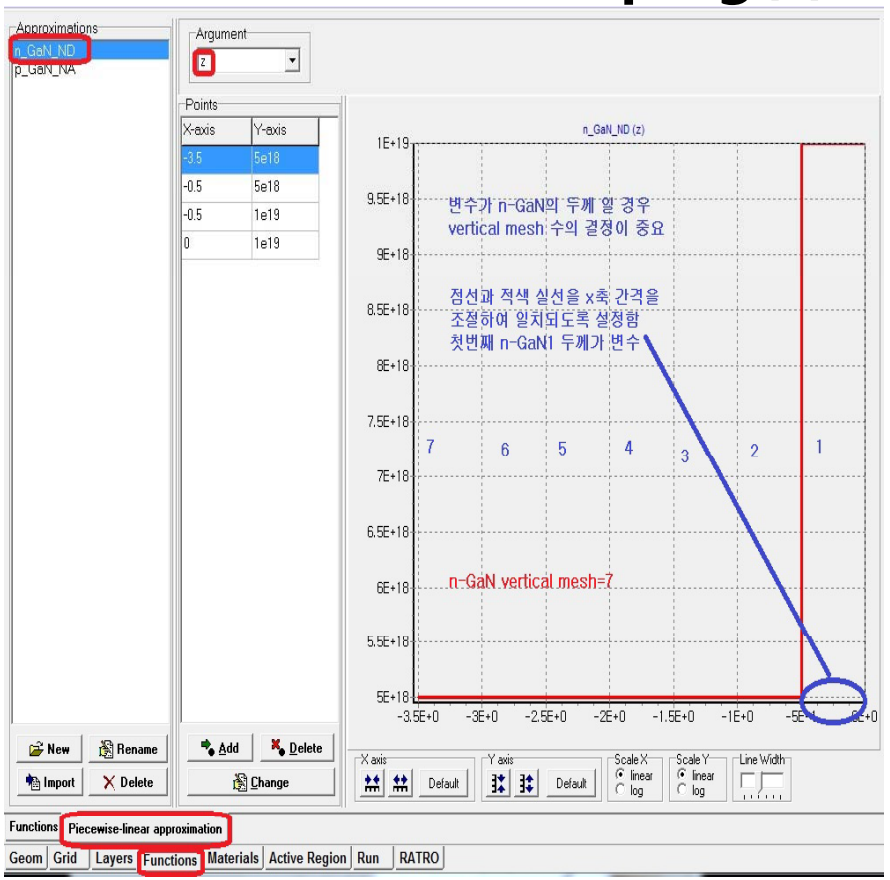
n-GaN profile

Thickness(-z)	E_Mobility(z,T)	Doping(z)
Z=0		
n-GaN1=0.5um	Mob=100*(300/T)	1e19
n-GaN2=3.0um	Mob=120*(300/T)	5e18

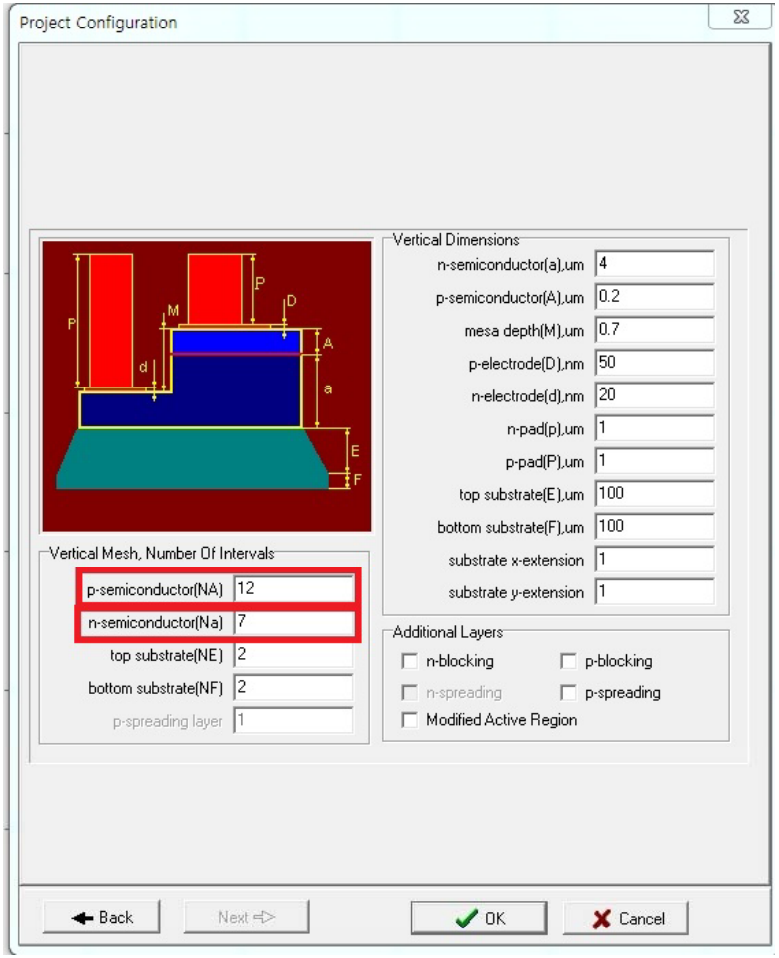
Function tab in mobility(z,T)

```
If (z<0) and (z>-0.5) then
   e_mob=100*(300/T);
If (z<-0.5um) then
   e_mob=120*(300/T);
Result=e_mob;
```

Piecewise tab in doping(z)

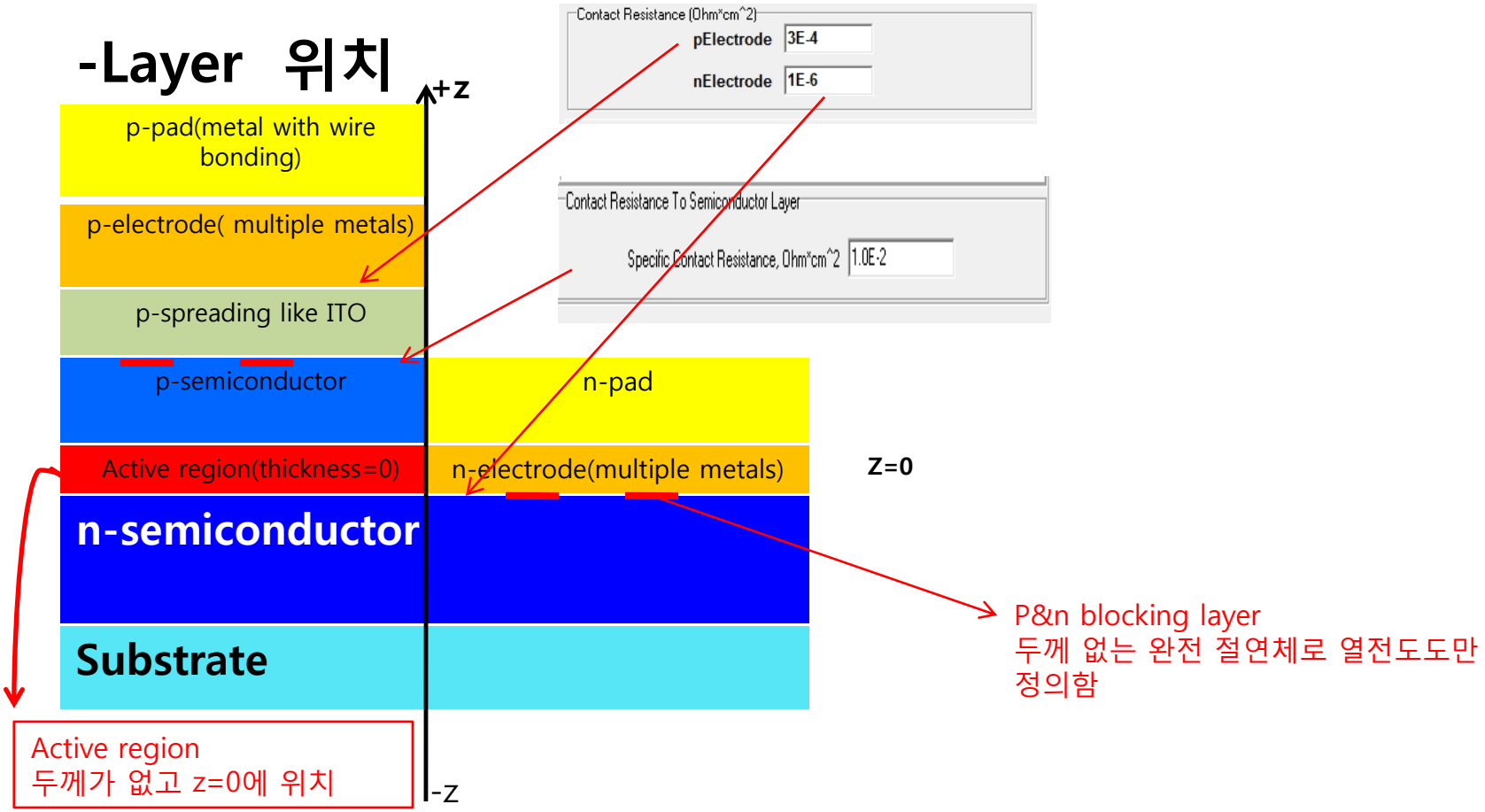


2-3-3. Vertical Mesh



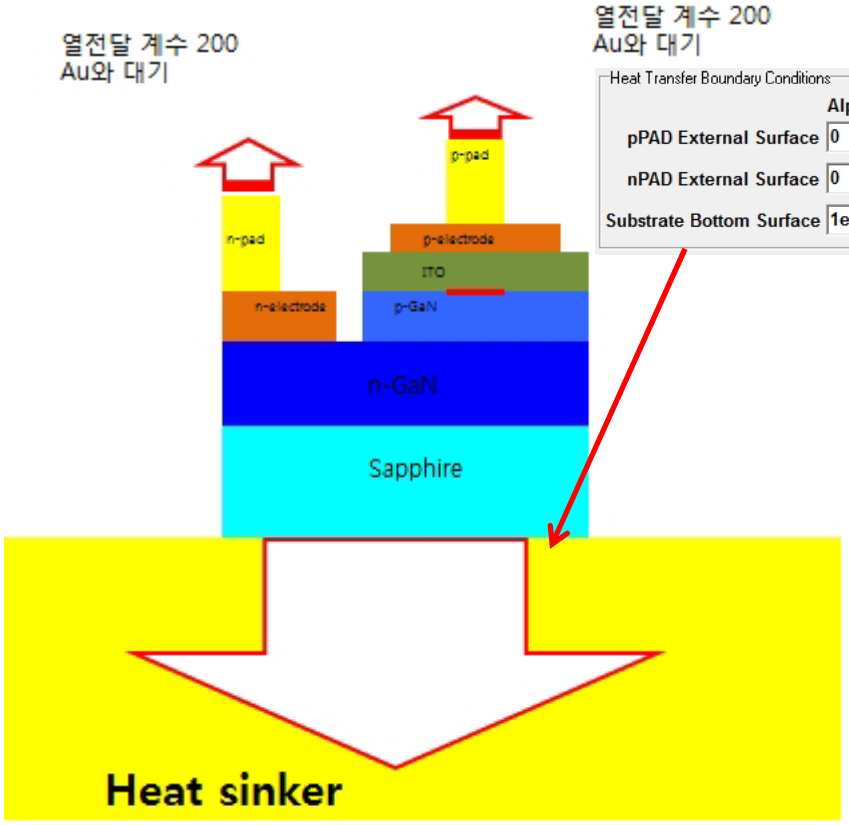
- Computation=Planar grids X vertical mesh
- Vertical mesh 수의 증가는 막대한 계산시간이 필요함으로 vertical mesh의 증가가 계산결과에 영향을 미치는 경우에만 사용을 권장
- 시뮬레이션 변수가 p-GaN 또는 n-GaN의 두께가 아닐 경우 p-GaN(3) and n-GaN(5)를 권장함

2-3-4. p&n 접촉 저항

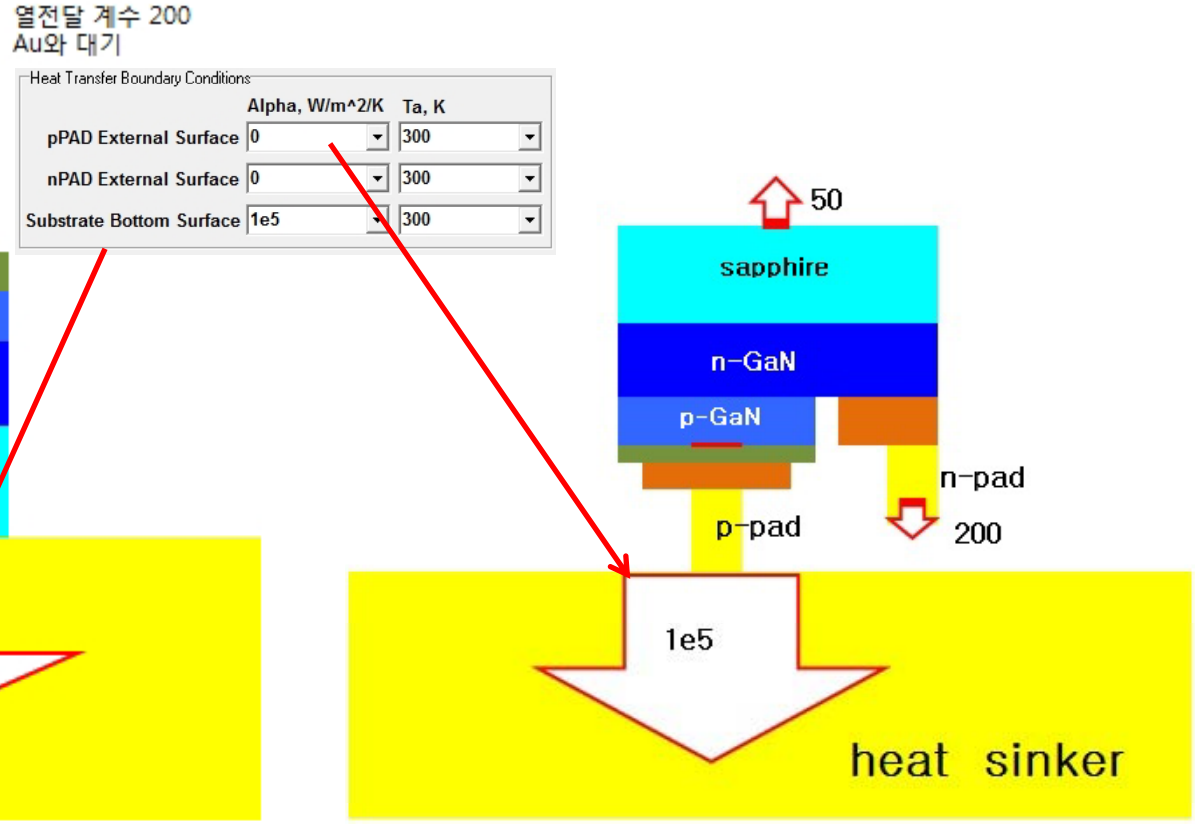

-Layer 위치
+z
p-pad(metal with wire bonding)
p-electrode(multiple metals)
p-spreading like ITO
p-semiconductor
n-pad
Active region(thickness=0)
n-electrode(multiple metals)
Z=0
n-semiconductor
Substrate
-z
Active region
두께가 없고 z=0에 위치
Contact Resistance (Ohm*cm^2)
pElectrode 3E-4
nElectrode 1E-6
Contact Resistance To Semiconductor Layer
Specific Contact Resistance, Ohm*cm^2 1.0E-2
P&n blocking layer
두께 없는 완전 절연체로 열전도도만 정의함

2-3-5. 열 전달 계수

수평형 일반칩

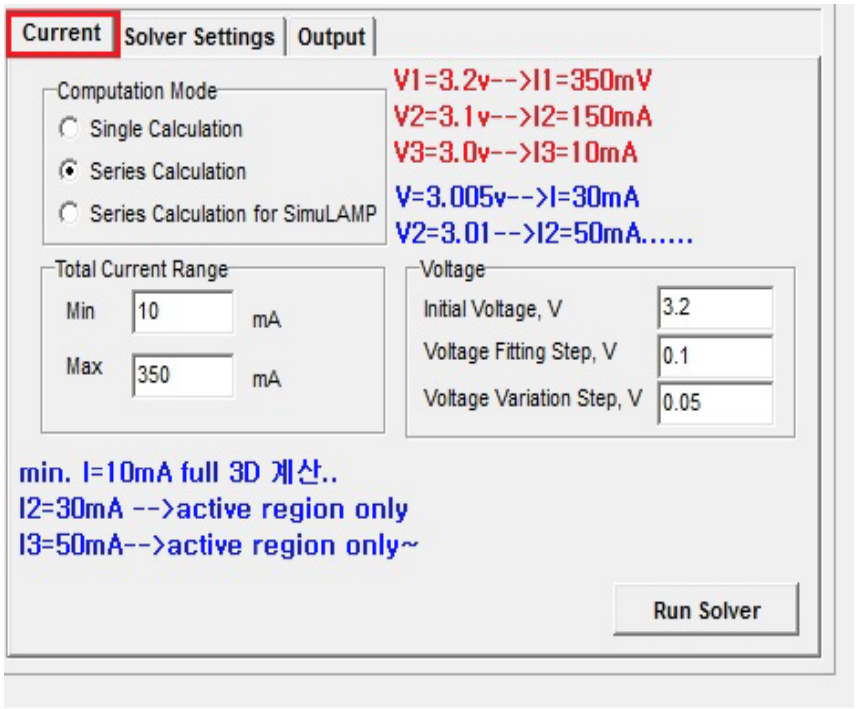


수평형 플립칩

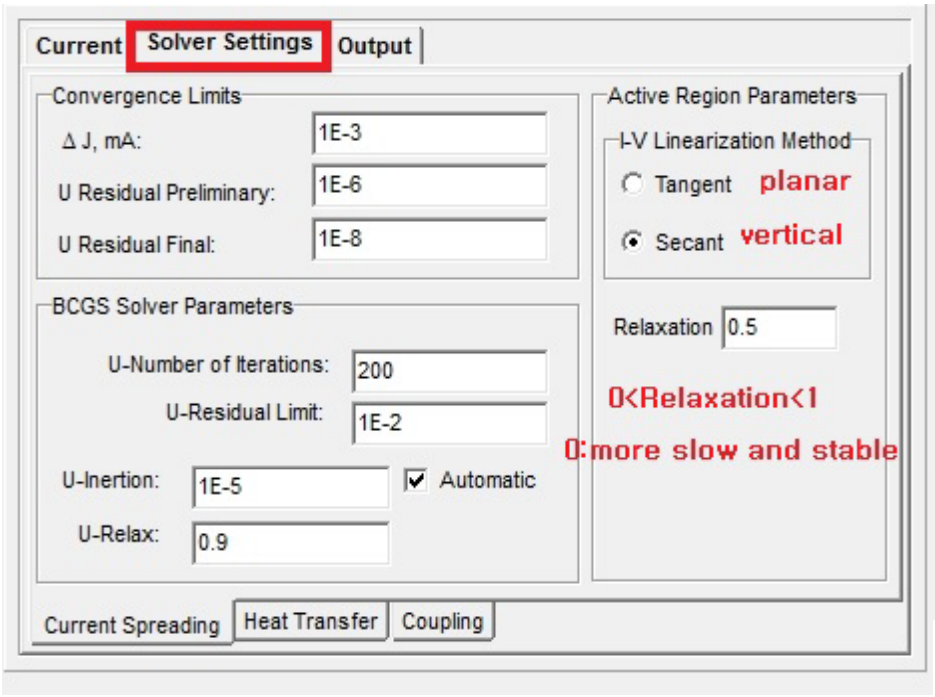


2-4. Computation mode

Series calculation



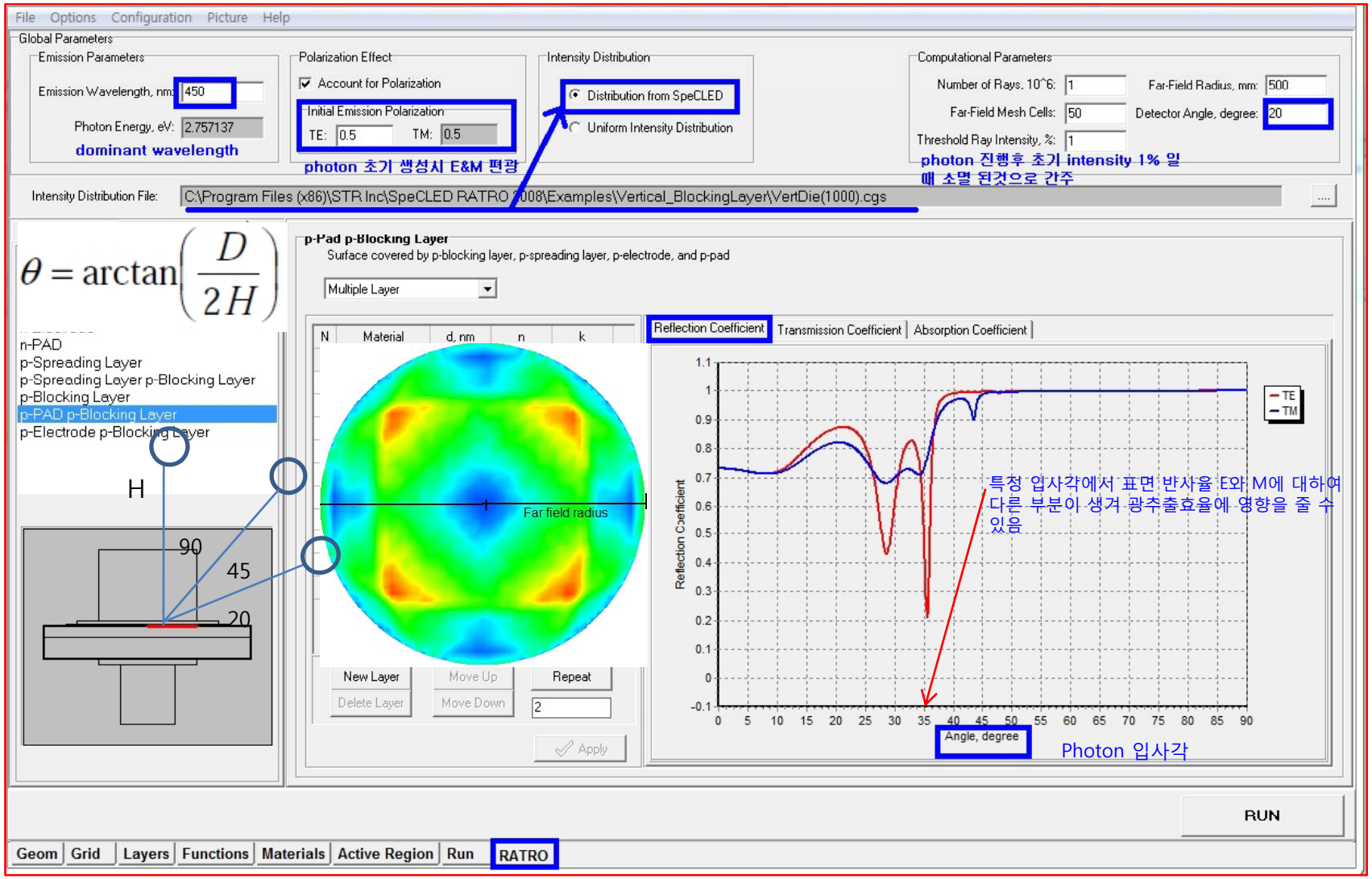
Solver setting



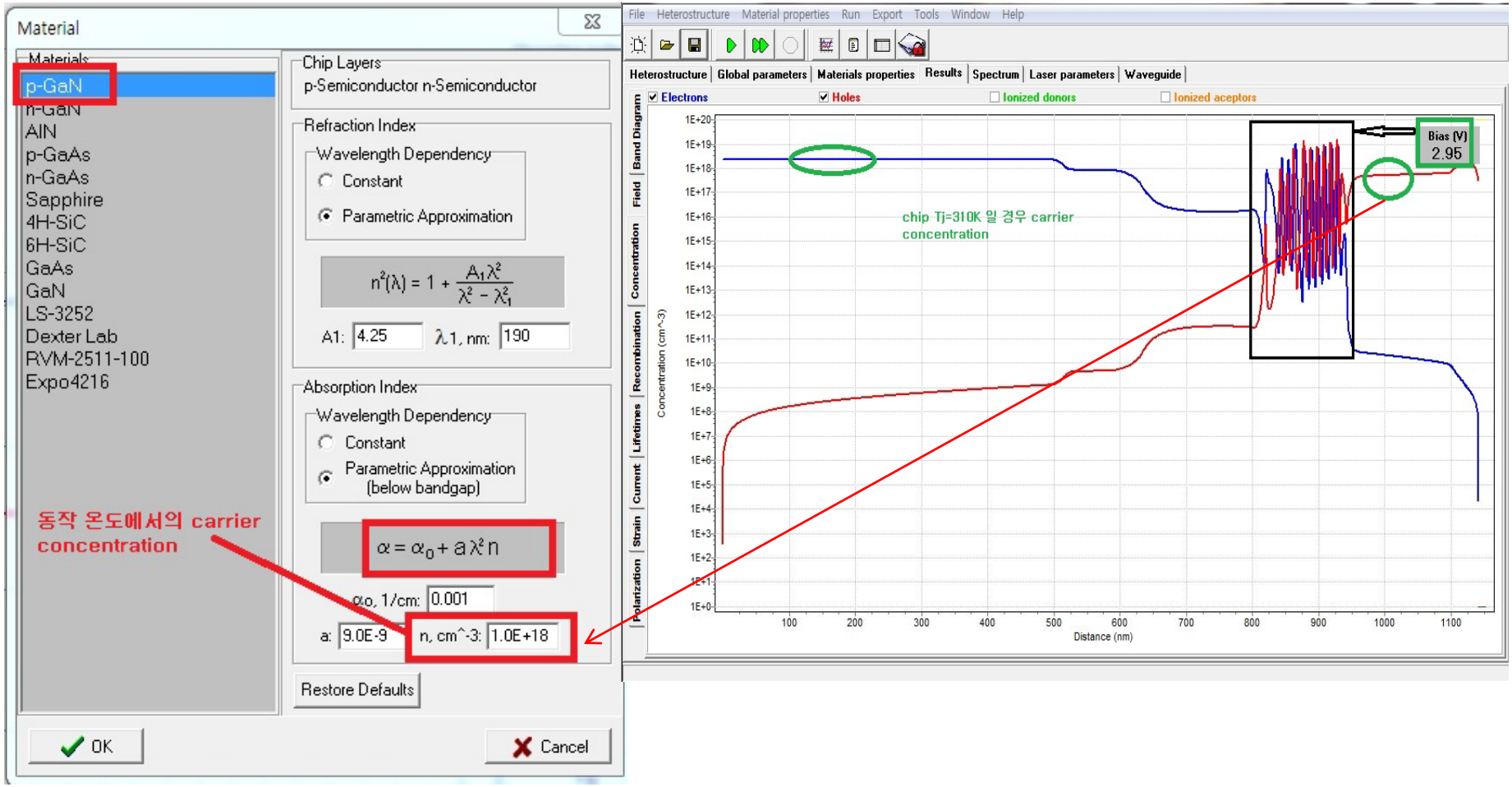
3. RATRO

- 3-1. Global parameters
- 3-2. Bulk Properties 정의
- 3-3. Surface Properties 정의

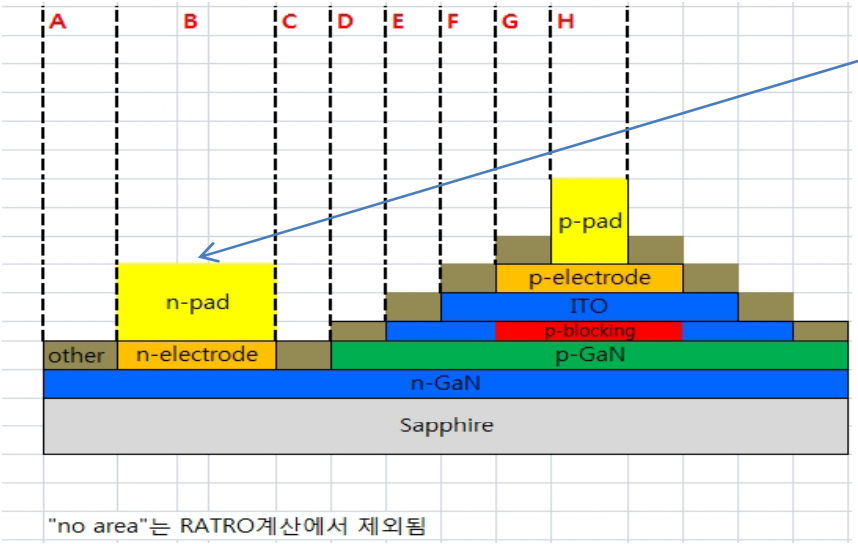
3-1 Global parameters



3-2 Bulk properties



3.3 Surface properties



"no area"는 RATRO계산에서 제외됨

1. "B"와 같이 n-pad=n-elec. 영역이 같은 경우 n-electrode 정의할 필요 없고, n-pad를 Multiple 선택하여 n-electrode 함께 묘사함

	Surface properties	Explanation
D	p-semiconductor	Free surface of p-semiconductor
G	p-electrode	Surface covered by p-spreading layer and p-electrode
no area	p-pad	Surface covered by p-spreading layer and p-electrode and pad
A	n-semiconductor	Free surface of n-semiconductor
no area	n-electrode	Surface covered by n-electrode only
B	n-pad	Surface covered by n-electrode and n-pad
	substrate bottom surface	
	hetero-structure/substate interface	
	substrate sidewall1	
	substrate sidewall2	
F	p-spreading layer	Surface covered by p-spreading layer only
F	p-spreading-p-blocking layer	Surface covered by p-blocking layer and p-spreading layer and not covered by p-electrode or pad
E	p-blocking layer	Surface covered by p-blocking layer only
H	p-pad p-blocking layer	Surface covered by p-blocking layer, p-spreading layer, p-electrode, and p-pad
G	p-electrode p-blocking layer	Surface covered by p-blocking layer, p-spreading layer, and p-electrode, not covered by p-pad

-시뮬레이션 순서-

- 1. SiLENSe:
  -입력: "Hetetrostructure", "Global parameter",
  -계산 모드: Series calculation for SpeCLED
  -생성 결과 파일: =>"~T_300.sct", "~T_320.sct", "~T_350.sct"

2. SpeCLED: 칩구조 입력
   "Active region"탭에서 1번 결과 생성파일 ".sct" 파일 온도 별로 로드

3. RATRO
   "Global parameter(Uniformity intensity 선택)"->"Bulk properties"→"Surface properties"→Run
   결과: LEE 계산

4. SpeCLED "Run"탭에 LEE(user input에 3번 결과 입력) 계산
   결과: ~(mA).cgs 파일

5. RATRO "intensity distribution from SpeCLED" 모드 선택→4번 .cgs 파일 선택
   "Run" 실행-→최종 RATRO 결과 ~(mA)_rtr.cgs 생성