



# SpeCLED

Spreading of Current in Light Emitting Diodes

Software for 3D Modeling of  
Current Spreading and Temperature Distribution in LED Chips

## Physics Summary

Version 4.12



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## 1 Overview

**SpeCLEd** is a software tool for design and optimization of LED layout. It performs 3D coupled simulation of the current spreading and heat transfer in LED dice and provides the following information:

- 3D distributions of the electric potential, current density, and temperature in LED die
- 2D distributions of the p-n junction bias, current density, internal quantum efficiency, and temperature in the active region plane
- I-V characteristic, series resistance, external quantum efficiency and wall-plug efficiency

**SpeCLEd** is a part of **SimuLED** package for complex analysis and optimization of LEDs, which consists of three tools:

- **SiLENSe** – 1D simulator of carrier injection and light generation in wurtzite III-N and II-O LED/LD heterostructures
- **SpeCLEd** – 3D simulator of current spreading and heat transfer in LED dice
- **RATRO** – 3D ray-tracing analyzer of light propagation and extraction in LED dice

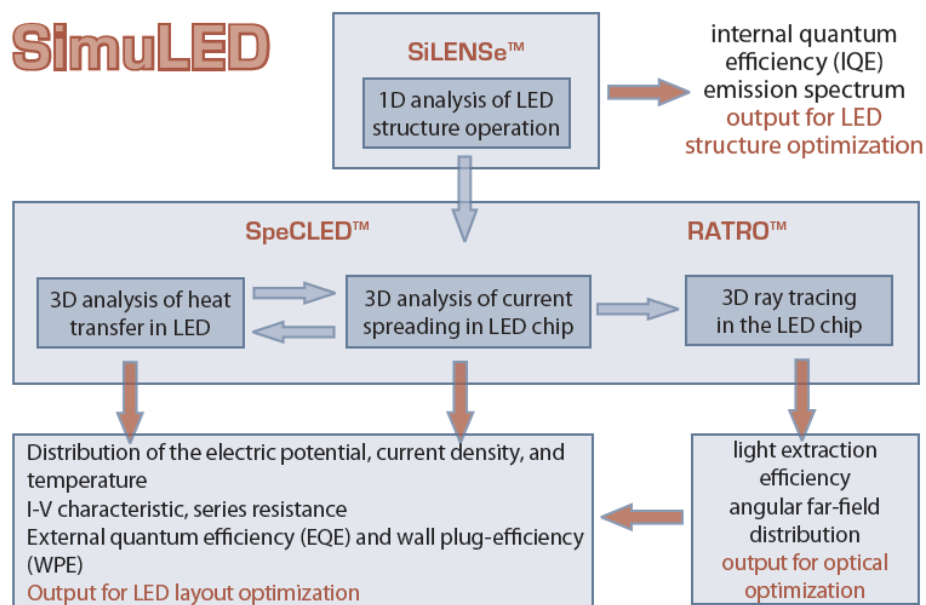


Fig. 1. **SimuLED** structure.

## 2 Current Spreading in an LED Die

### 2.1 Basic Equations

A LED heterostructure is considered as a set of following layers: substrate, thick n-type semiconductor layer, active region, thick p-type semiconductor layer, metallic electrodes and pads, as well as additional layers like current spreading layer (ITO) and current blocking layer (thin insulator layer). To simulate the current spreading in an LED die, a hybrid 1D/3D approach is used. Electrically neutral p- and n-regions are chosen in the die where drift is the dominant mechanism of the carrier transport and the electron-hole recombination is suppressed (see Fig. 2 as an example). Current spreading in these regions is described by the Ohm law.

The electrically neutral regions are separated by a thin active layer that includes a single or multiple quantum well (MQW) with adjacent space-charge regions. The active layer is considered as a non-linear resistor, distributed in the p-n junction plane, with the vertical current density  $j_z$  locally controlled by the voltage (bias)  $U_b$  induced at the top and bottom interfaces of the layer.

In **SpeCLED**, the current spreading in the neutral regions of the LED die is considered within a 3D approach, while the relationship between  $j_z$  and  $U_b$  can be found from 1D computations by **SiLENSe** package or defined by the user.

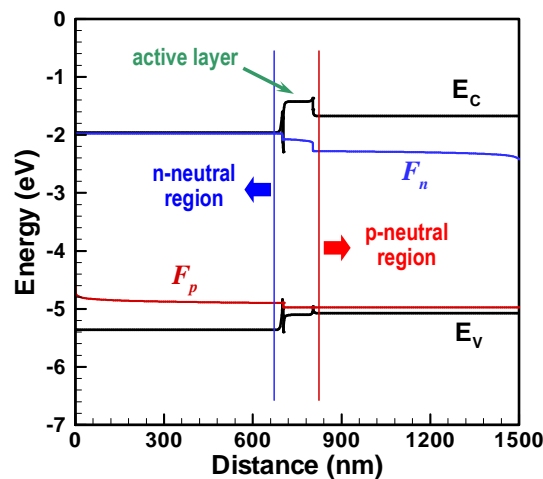


Fig. 2

Choice of quasi-neutral regions and active layer in an LED heterostructure.  $E_c$  and  $E_v$  denote the conduction and valence band edges, respectively.  $F_n$  and  $F_p$  are the quasi-Fermi levels.

The current density  $\mathbf{j}$  in every semiconductor block obeys the equation

$$\mathbf{j} = (\hat{\sigma} / q) \nabla F \quad , \quad \hat{\mu} = \begin{pmatrix} \mu_{\perp} & 0 & 0 \\ 0 & \mu_{\perp} & 0 \\ 0 & 0 & \mu_{\parallel} \end{pmatrix} \quad (1)$$

where  $\hat{\sigma} = q\hat{\mu}N_i^{\pm}$  is the conductivity tensor of the epilayer,  $q$  is the electron charge,  $\hat{\mu}$  is the mobility tensor accounting for possible difference between the in-plane ( $\mu_{\perp}$ ) and normal ( $\mu_{\parallel}$ ) carrier mobilities,  $N_i^{\pm}$  ( $i = D, A$ ) is the ionized impurity (donor or acceptor) concentration equal to the carrier (electron or hole) concentration in the layer due to the electric neutrality, and  $F$  is the quasi-Fermi level of the respective carriers. As the electric neutrality is assumed in every epilayer of the die, except for the active layer, the quantity  $\Phi = F - E_s + q\phi$ , where  $E_s$  indicates the conduction or valence band edge and  $\phi$  is the electric potential, is constant throughout the layer. This means that  $\nabla F = -q\nabla\phi$ , i. e. Eq.(1) actually represents the Ohm law.

The ionized impurity concentrations can be found from the electro-neutrality conditions. For electrons

$$N_D^+ = N_C \cdot F_{1/2}(\Phi / kT) = \frac{N_D}{1 + g_D \exp\left(\frac{\Phi + E_D}{kT}\right)} \quad (2)$$

where  $N_C$  is the density of states in the conduction band,  $g_D$  is the electron degeneracy factor,  $E_D$  is the donor ionization energy, and  $F_{1/2}(\xi)$  is the Fermi integral. For holes, respectively

$$N_A^- = N_V \cdot F_{1/2}(-\Phi / kT) = \frac{N_A}{1 + g_A \exp\left(\frac{E_A - \Phi}{kT}\right)} \quad (3)$$

where  $N_V$  – is the density of states in the valence band,  $g_A$  is the hole degeneracy factor, and  $E_A$  is the acceptor ionization energy. Eqs. (2)-(3) allow determination of  $\Phi$  in each of the epilayers and then calculation of the respective electric conductivity as a function of the doping level and temperature.

Since the carrier recombination is negligible in the electrically neutral regions,  $\nabla \cdot \mathbf{j} = 0$ , which produces the final equation for the quasi-Fermi level

$$\nabla \cdot (\hat{\sigma} \nabla F) = 0 \quad (4)$$

The boundary conditions to Eq.(4) depend on the interface type as considered below.

## 2.2 Internal Interfaces with zero resistance

The boundary conditions at the interfaces with no resistance are as follows

$$F_1 = F_2 \quad (5)$$

$$\mathbf{n} \cdot (\hat{\sigma}_1 \nabla F_1 - \hat{\sigma}_2 \nabla F_2) = 0 \quad (6)$$

where  $\mathbf{n}$  is the normal vector to the interface. These boundary conditions are applied for the interface between the substrate and the epilayers.

## 2.3 Active Layer

The transport and recombination processes inside the active layer of an LED are not simulated by the **SpeCLED** software. For this purpose, 1D modeling accounting for the complex internal structure of the active layer can be employed, by using, for instance, the **SiLENSe** package. As a result, the dependence of the vertical current density  $j_z$  upon the bias  $U_b$  applied to the active layer is generated or defined by user via parametric approximations. The **non-linear dependence**  $j_z(U_b)$  is then used to produce the boundary conditions relating the quasi-Fermi levels and their gradients at the top ( $F_p$ ) and bottom ( $F_n$ ) active layer interfaces

$$\mathbf{n} \cdot \hat{\sigma}_p \nabla F_p = \mathbf{n} \cdot \hat{\sigma}_n \nabla F_n = j_z(F_n - F_p) \quad (7)$$

It is assumed in Eq. (7) that the normal  $\mathbf{n}$  is directed from p- to n-material and that  $U_b = F_n - F_p$  (see Fig. 2).

## 2.4 Interface between Dielectric and Semiconductor Layers

Due to absence of the electric current in a dielectric film, the following boundary conditions should be met at a dielectric/semiconductor interface

$$\mathbf{n} \cdot \nabla F = 0 \quad (8)$$

## 2.5 Interface between Heterostructure and Metal Electrode (Ohmic Contact)

Let  $F_s$  и  $F_m$  be the quasi-Fermi levels of electrons or holes in the semiconductor material or metal film. Then the boundary conditions accounting for the specific contact resistance  $\rho_c$  read

$$\mathbf{n} \cdot \hat{\sigma}_s \nabla \varphi_s = (F_m - F_s) / \rho_c \quad (9)$$

where  $\hat{\sigma}_s$  is the semiconductor conductivity. It is assumed in Eq.(9) that the normal  $\mathbf{n}$  is directed from semiconductor to metal.

The same model is used for the ITO/semiconductor and ITO/metal interfaces.

## 2.6 Current Spreading in Thin Metallic Electrodes and Pads

It is assumed that the Fermi-level potential variation across a thin metal film is negligible and that the electric current flows mostly in the film plane. In this case one can operate with the current density averaged over the film cross-section,  $\mathbf{j}_m$ . Integration of the continuity equation for the current density across the film provides the equation  $h \nabla_2 \cdot \mathbf{j}_m = j_{out}$ , where the subscript '2' denotes the 2D operator, while  $j_{out}$  is the current outgoing from the metal film in a normal direction described in Sec. 2.5.

Thick "wire" areas are assumed to have constant electric potential that equals zero for n-wire and forward voltage applied to the LED for p-wire.



### 3 Heat Transfer Model

#### 3.1 Basic Equations

Heat transfer in the chip layers is described by the following equation:

$$-\nabla(\lambda\nabla T) = q \quad (10)$$

where  $T$  is the temperature,  $\lambda$  is the thermal conductivity and  $q$  is the local heat source dependent on the current density.

#### 3.2 Boundary Conditions

LED dice is suggested to be surrounded by the medium with poor thermoconductivity (air or epoxy). So all the external surfaces are assumed to be adiabatic, except to the following ones which are usually used for heat removal:

- External surface of the substrate (for conventionally mounted LEDs).
- External surfaces of the pad contacts (for flip-chip mounted LEDs)

The heat flux at these surfaces is related to the temperature  $T$  as

$$q = \alpha(T_a - T) \quad (11)$$

where  $\alpha$  is a heat transfer coefficient and  $T_a$  is an ambient temperature. Parameters  $T_a$  and  $\alpha$  should be assigned by the user. The surfaces temperature is determined by balancing the external and internal heat fluxes. Eq. (11) assumes the following limiting cases:

- $\alpha \rightarrow \infty$ . Isothermal boundary,  $T = T_a$
- $\alpha = 0$ . Adiabatic boundary,  $q = 0$

#### 3.3 Heat Sources and LED Efficiency

The volumetric heat power due to joule heat sources can be found as

$$Q_1(x, y, z) = j^2(x, y, z) / \sigma(x, y, z) \quad (12)$$

where  $j(x, y, z)$  and  $\sigma(x, y, z)$  are three-dimensional current density and specific electric conductivity distribution in the LED die. The power dimensionality is  $[Q_1] = \text{W}/\text{cm}^3$ , current dimensionality is  $[j] = \text{A}/\text{cm}^2$ , and conductivity dimensionality is  $[\sigma] = (\Omega \cdot \text{cm})^{-1} = \text{S}/\text{cm}$ .

The surface heat power released in the LED active region is calculated as a difference between the total electrical power released in the active region and the power converted into light. Assuming that the most of absorption of the emitted light occurs also in the active region because of its narrow-gap layers, we can express the heat source as

$$q_0(x, y) = j_z(x, y) \cdot U_b(x, y) - \frac{j_z(x, y)}{q} \cdot \hbar\omega \cdot \eta_{\text{int}}(x, y) \cdot \eta_{\text{ext}} \quad (13)$$

where  $j_z(x, y)$  is the local density of current flowing through the p-n junction,  $U_b(x, y)$  is the local bias on the p-n junction,  $\eta_{\text{int}}(x, y)$  is local internal quantum efficiency, and  $\eta_{\text{ext}}$  is the light extraction efficiency. Generally, energy of the emitted quant  $\hbar\omega$  depends on  $x$  and  $y$  due to wavelength variation with the current, but this effect can be not so important for the heat release calculation. If characteristics of the active region are imported into **SpeCLED** from **SiLENSe**,  $\hbar\omega$  is found from the chip spectrum computed by **SiLENSe**. Otherwise it is calculated from the emission wavelength assigned by the user. The surface heat source dimensionality is  $[q] = \text{W}/\text{cm}^2$ .

On the n-electrode / n-contact layer and p-electrode / p-contact layer interfaces the surface heat power release  $q_n$  and  $q_p$ , respectively, are found as

$$q_n = \rho_n \cdot j_z^2 \quad , \quad q_p = \rho_p \cdot j_z^2 \quad (14)$$

where  $\rho_n$  and  $\rho_p$  are the contact resistances.

The total power of radiation extracted from the LED chip is defined as

$$W_{\text{rad}} = \frac{\hbar\omega}{q} \eta_{\text{ext}} \cdot \int dx dy \cdot j_z(x, y) \eta_{\text{int}}(x, y) \quad (15)$$

Then the chip wall-plug efficiency can be found as

$$\eta_{\text{WP}} = W_{\text{rad}} / (I \cdot U) \quad (16)$$

where  $U$  is the total bias applied to the chip and  $I$  is the total current.

The external quantum efficiency of a LED chip is defined as the ratio of the number of light quanta extracted from the die to the number of electron-hole pairs injected into the heterostructure. It can be found as

$$\eta_Q = \frac{\eta_{\text{ext}}}{I} \cdot \int dx dy \cdot j_z(x, y) \eta_{\text{int}}(x, y) \quad (17)$$

## 4 Manual Input of I-V Characteristics of Active Region

When **SpeCLED** is used as a part of the whole **SimuLED** package, the heterostructure active region characteristics used as input data are normally generated by the **SiLENSe** code. In addition, the **SpeCLED** allows user to specify the required active region parameters manually using the graphical user interface. The approximations used to specify the active region current-voltage characteristics and internal quantum efficiency are described below.

### 4.1 Relationship between the Bias and Current Density

The relationship between the current density  $j$  and the bias  $U_b$  applied to the p-n junction at temperature  $T$  is defined by the expression followed from the Shockley's diode model:

$$U_b = \frac{mkT}{q} \ln \frac{j + j_0 \exp(-E_G / kT)}{j_0 \exp(-E_G / kT)} + j\rho_A \quad (18)$$

Here,  $q$  is the electron charge and  $k$  is the Boltzmann constant. In addition, this approximation involves the following parameters:

- $j_0$  – saturation current density
- $m$  – non-ideality factor. Typical values can be in the range of 1.0 – 2.0. By default,  $m = 1$
- $\rho_A$  – series resistance of the active region
- $E_G$  – band gap of the used material (eV). For InGaN LEDs, typical values of  $E_G$  can be in the range of 2.5 - 3.5

As an example, Fig. 3 presents the corresponding I-V characteristics for three temperature values for the following parameters:

$$j_0 = 6 \times 10^{18} \text{ A/cm}^2, E_G = 3.4 \text{ eV (GaN)}, \rho_A = 10^{-5} \text{ } \Omega \cdot \text{cm}^2.$$

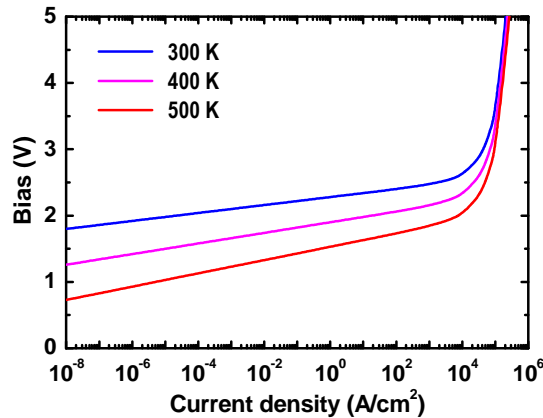


Fig. 3

The parameters  $m$  and  $j_0$  are largely responsible for the low-current region of the  $j(U_b)$  characteristic. So, they can be fitted by considering the low-current portion of the actual I-V characteristic of an LED. The parameter  $E_G$  determines the turn-on voltage of the LED. So, its value can be adjusted to the experimentally measured turn-on voltage. The parameter  $\rho_0$  determines the behavior of the  $j(U_b)$  curve under high-current conditions. Note that  $\rho_0$  is series resistance of the p-n junction only, not the total series resistance of a chip.

## 4.2 IQE as a Function of Current Density

The relationship between internal quantum efficiency (IQE)  $\eta$  and current density  $j$  is approximated using a parametric setting as follows:

$$j(N) = qd \cdot \left( N / \tau + BN^2(T/T_0)^{-3/2} + CN^3(T/T_0)^\gamma \right) \quad (19)$$

$$\eta(N) = (qd / j) \cdot BN^2(T/T_0)^{-3/2} \quad (20)$$

Here:

- $N$  is the non-equilibrium carrier concentration in the active region
- $q$  is the electron charge
- $d$  is the active region thickness (in the case of MQW structure it is the total thickness of all quantum wells)
- $\tau$  is the non-radiative lifetime (typically equal to 20-100 ns)
- $B$  is the radiative recombination rate constant at  $T_0$  (typically equal to  $2-3 \times 10^{-11} \text{ cm}^3 \text{ s}^{-1}$ )
- $C$  is the Auger recombination coefficient at  $T_0$  (typically equal to  $1-10 \times 10^{-31} \text{ cm}^6 \text{ s}^{-1}$ )
- $T_0$  is the room temperature

This parameterization procedure produces the behavior of  $\eta(j)$  similar to that observed experimentally (see Fig. 4) and allows much more easier parameter fitting to measured external efficiency versus forward current.

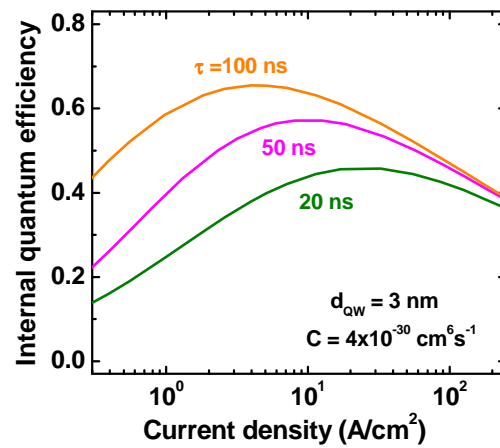


Fig. 4