SpeCLED

Spreading of Current in Light Emitting Diodes

RATRO

RAy-TRacing SimulatOr of Light Propagation

Software for 3D Modeling of
Current Spreading, Temperature Distribution and
Light Extraction in LED Chips

Getting Started

Version 4.12

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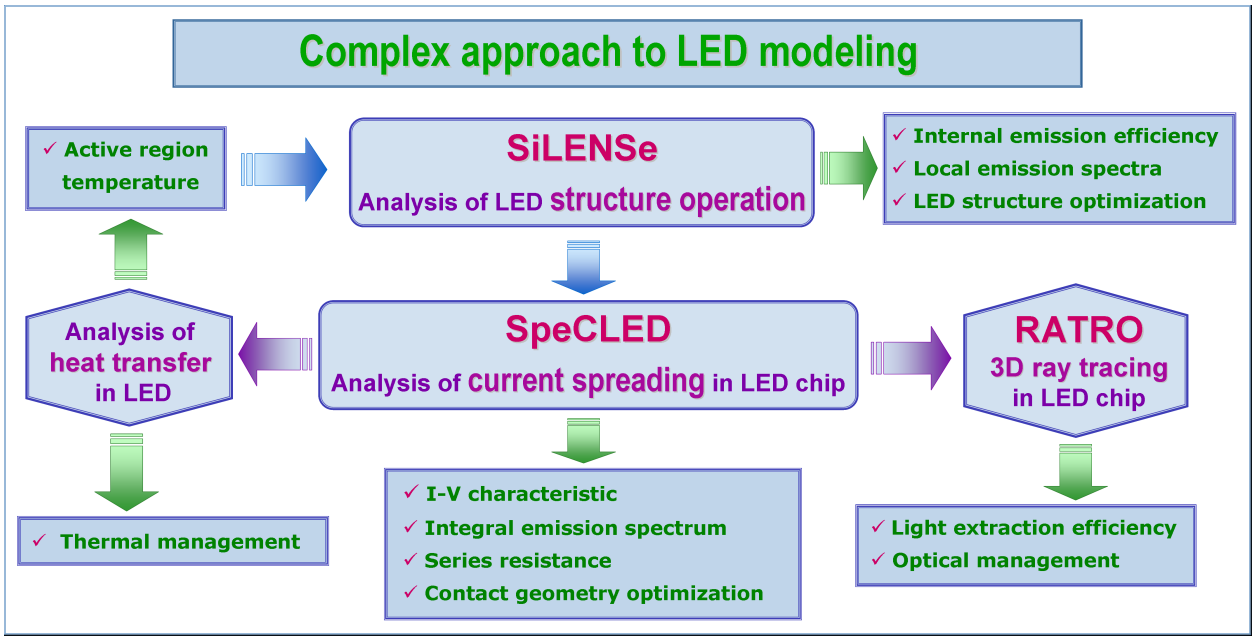
Table of contents

1 Introduction

Both **SpeCLED** and **RATRO** are modules of the software package **SimuLED** that implements an advanced approach to device modeling and provides device engineers with exhaustive information about LED operation. **SpeCLED** provides a self-consistent solution of a coupled problem of the current spreading and heat transfer in LED chips, while **RATRO** is designed for modeling the light extraction from LED chips using ray-tracing approach. The principal scheme of **SimuLED** operation is shown below.



1.1 Configurations

SpeCLED 2008 and **RATRO 2008** share a common graphical user interface which allows the user to specify the 3D geometry and physical parameters of the LED materials and surfaces and run the computations. The software can be supplied with one of the following configurations:

- **SpeCLED** only
- **RATRO** only
- **SpeCLED & RATRO**

1.2 SpeCLED Model and Results

SpeCLED provides 3D solution of coupled heat transfer and current spreading problems for in planar and vertical dice including the following processes:

- current spreading in n- and p- semiconductor layers, substrate, metal electrodes and pads, and ITO spreading layer
- non-linear resistance of the active region, which can be imported from calculations made by the **SiLENSe** software or specified manually by the user
- Heat transfer in n- and p-contact layers, electrodes pads and substrate with boundary conditions accounting for the heat sink on external pads or substrate surfaces.

All the material properties can depend on both coordinates and local temperature.

The results of modeling by **SpeCLED** include the following:

- Electric potential distribution in the whole die
- Current density distribution in the whole die
- Light emission intensity distribution across the p-n junction plane
- Temperature distribution in the whole die
- I-V characteristics of the LED
- Total current
- Wall-plug efficiency

The results obtained by **SpeCLED** can be used by **RATRO** software to calculate the light extraction efficiency and the radiation pattern of emitted light.

1.3 RATRO Model and Results

RATRO provides coupled solution of ray-tracing and light extraction problems, accounting for:

- Non-uniform light emission from the active region, which is found by solving the current spreading problem using **SpeCLED**. **RATRO** can also be used without **SpeCLED**, in this case uniform light emission from the active region is assumed.
- Absorption in semi-transparent materials (GaN contact layers, wafer, thin metal electrodes)

- Light polarization
- Light reflection and refraction at the external chip surfaces and heterostructure-wafer interface
- Light interaction with thin multiple layer metal electrodes
- Light interaction with patterned surfaces. Regular rectangular and hexagonal facets are supported.

The ray tracing computational domain in **RATRO 2008** includes the n- and p- semiconductor layers and the substrate. Electrodes, pads, spreading and blocking layers are not considered as bulk objects of the computational domain. Instead, their effect on the light extraction is included through the different conditions fro light interaction with different surfaces like a free semiconductor surface, a surface covered by electrode, etc. Several types of surface models is supported including multiple layer reflective or anti-reflective coatings, DBR, patterned surfaces, etc.

The results of modeling by **RATRO** include the following:

- Integral light extraction efficiency of an LED chip for both top and bottom hemispheres
- 2D light intensity distributions for far-field and near-field emission
- 3D light visualization of light intensity distributions for near-field emission
- Radiation patterns

2 Installation

This section describes the procedure of the installation of **SpeCLED & RATRO** software on a PC running Windows XP/Vista/7. During the installation, the user should assign the home directory to install the package. Installation wizard, in particular, creates a shortcut to the **SpeCLED & RATRO** shell, **SimuLEDView** and manual files and assigns associations for the **SpeCLED & RATRO 2008** project files (*.dvx) to the shell, results files (*.cgs) to the **SimuLEDView** and residual plotter files (*.spl) to **SpeCLED** solver.

3 Registration

SpeCLED & RATRO is supplied on terms of single-node license using dongle key protection. The program is delivered with a dongle key that should be plugged in a USB port on the PC where **SpeCLED & RATRO** will be used. Information on the license expiration date is available in the *About* dialog window. The software may be installed on several PCs, while the software operates only if the dongle key is plugged in. Two types of dongle keys are used: HASP and Senselock, while their operation is nearly the same for user's.

When the license expires, the user has to contact STR Group by e-mail on the issue of the license prolongation. To prolong the license, the user should use the license manager (`License.exe` file in the *SpeCLED & RATRO* home directory) program which is available via the **License Manager** item in the *SpeCLED & RATRO* group in the Windows *Programs* menu. This can be done as follows:

- Plug in the dongle key
- Start the **License Manager**
- Press **Make Key** button to generate license request. It is a string for HASP dongle and a file for Senselock dongle.
- Send the generated license request (string or file) to STR by e-mail simuled-support@str-soft.com
- After the answer from STR is received including the license string (HASP dongle) or license file (Senselock dongle), start the **License Manager** and press **Accept Key** button. One will need paste the license string (HASP dongle) or browse for the license file (Senselock)
- Close the **License Manager**
- Open **SpeCLED & RATRO**

4 Getting Started with SpeCLED

4.1 Operation Overview

Operation of the user with **SpeCLED** includes the following:

- Selection of the chip configuration. Four predefined types of configurations are available: planar and vertical dies which may include substrate or not.
- Assignment of the vertical dimensions of the chip elements and parameters of the substrate shape
- Drawing of the die geometry in planar top view in the Graphical User Interface, which includes drawing the contours and assigning the constructive elements of the die.
- Specification of the die geometry by assigning the drawn contours to the respective chip elements.
- Building the planar computational grid. For a vertical die, independent grids may be generated in n- and p- sides of the die.
- Specification of the physical characteristics of all used materials. The material characteristics can be assigned using a predefined material database.
- Specification the characteristics of the active region, which can be done manually or by loading data generated by the **SiLENSe** software tool included into the **SimuLED** software package along with **SpeCLED.**
- Assigning the boundary conditions.
- Running the computations. Computations may be run either for a single value of the total current in the chip or for a range of current variation resulting in calculation of the chip I-V characteristics.
- Visualization of the obtained results in **SimuLEDView**

4.2 Chip Configuration

First, the user should select the basic type of the LED geometry. The current version of **SpeCLED** supports 4 die configurations:

- Planar die (one-side electrode configuration). N-electrode and p-electrode are on the same side of the die, so that n-contact window is etched in the p-semiconductor layer.

- ✓ With a conducting or insulating substrate. Substrate is included into the computations.
- ✓ Without a substrate.

- Vertical die (two-side electrode configuration). N-electrode and p-electrode are on the opposite sides of the die.
  - ✓ With a conducting substrate. Substrate is included into the computations.
  - ✓ Without a substrate.

Specification of the chip geometry also includes prescription of optional die elements which may be included in the chip:

- n-blocking layer – insulating layer separating n-semiconductor layer and n-pad
- p-blocking layer – insulating layer separating p-semiconductor layer and p-pad
- p-spreading layer – a conductive layer between p-contact layer and p-electrode (for instance, ITO)

4.3 Geometry Specification

The next stage of a simulation is specification of the die geometry. For a planar die, the user has to draw one set of contours including all die elements. For a vertical die, the user has to draw two independent set of contours representing n-side and p-side of the die. However, external contours of the n- and p-side should match.

The planar geometry of each chip element should be represented as a set of boundaries forming a closed contour (or a set of contours) bounding the corresponding element. A boundary can represent either a line or an arc.

The drawing of the die geometry includes the following contours:

- n-semiconductor layer, which always represents the external die contour
- p-semiconductor layer area, which matches n-contact layer area in a vertical LED and has smaller area in case of a planar LED
- n- and p-electrodes inside the respective semiconductor layers
- n- and p- pads inside the respective electrodes
- n- and p- wire plates inside the respective pads
- n-blocking layer (if specified in the chip configuration)
- p-blocking layer (if specified in the chip configuration)

- p-spreading layer (if specified in the chip configuration)

Wire plates represent areas where wires are connected to and voltage is applied. In most cases, in particular in flip chip LEDs or in case of relatively thick pads, they match the pad areas. Implementation of wire plates as separate elements provides account of with considerable potential drop in thin pads when the contact area is smaller than the overall pad surface.

Note that substrate is not drawn along with the other chip elements. Two substrate geometries are supported:

- Flat substrate. The substrate geometry matches the external contour of the n-contact layer.
- Shaped substrate – a substrate with sloped side walls. The substrate geometry is parametrically specifies by enlargement parameters that define dimensions of the bottom substrate area.

Substrate enlargement parameters, as well as all vertical dimensions of the die, are assigned along with the chip configuration.

After drawing the contours the user should assign them to the respective chip elements. For each chip element the user should pick all closed contours which correspond to this element.

4.4 Meshing

To achieve a high efficiency and required flexibility in complex geometry treatment, the planar chip elements can be meshed by either structured (rectangular) or unstructured (triangular) computational grids generated by the grid generator incorporated into the code.

Note that generation of rectangular grid requires representation of the corresponding domain as a set of rectangles. If the actual geometry of a chip element is not rectangular but allows its fragmentation into a set of rectangles, this can be done using auxiliary lines. In this case the given chip element will be represented as set of several closed contours, all of which should be picked at the stage of specification of the geometry of the chip elements.

3D mesh is done automatically by the program using the specified 2D mesh and the data on the height of the corresponding chip elements. Vertical mesh density can be assigned by the user along with vertical die dimensions at the chip configuration specification.

Prior to the 2D meshing that is done automatically the user has to assign fragmentation parameters to all boundaries, defining the edges of mesh cells. This can be done either automatically or manually. In the automatic mode, the user should assign the mesh density that is applied to all boundaries. In the manual mode, fragmentation of each boundary can be assigned individually.

4.5 Material Properties

After specification of the die geometry, the user should load the materials used from another project file and assign the materials to the corresponding elements. If some materials are not contained in the supplied database, the user should first create a new material, specify its characteristics and then assign the material to the chip elements.

Generally, for each material one need specify the thermal and electrical conductivity. For the semiconductor materials, the electrical conductivity is specified through the common semiconductor parameters:

- Mobility in lateral and normal direction, $cm^2/(V \cdot s)$
- Dopant concentration, cm^{-3}
- Dopant activation energy, eV
- Electron Density of States, cm^{-3}
- g-factor

All parameters can be specified as functions of both temperature and coordinate, so that temperature dependence and non-uniform distribution of die layer characteristics are supported.

4.6 Active Region Characteristics

In addition to specification of the die geometry design and boundary conditions, the user should specify the I-V characteristics of the active region in the operating temperature range. This can be done as follows:

- Importing files generated by the **SiLENSe** software. These files contain data on the I-V characteristics at a set of temperatures and the emission spectra for all these temperatures in the wide range of voltage variation.
- Parametric approximation of the I-V and IQE characteristics
- Manual specification of I-V, IQE and spectral characteristics in a table format.

4.7 Isothermal and Coupled Computations

SpeCLED can be operated in different modes, so the user should specify the problems to be solved. The following options are available:

- *Isothermal Current Spreading*. The current spreading in isothermal die is only modeled. The die temperature is assumed to be constant and specified by the user.
- *Coupled Current Spreading and Heat Transfer*. In this mode, two problems are solved in a coupled formulation: current spreading in non-isothermal die and the heat transfer. So both the current effect on the heat transfer and the temperature non-uniformity effect on the current spreading are accounted for, providing a self-consistent solution.

4.8 Heat Transfer Problem

If the Heat Transfer problem is solved, the user should specify the boundary conditions at the following external boundaries of the die where heat sink is available:

- surfaces of n-pad wire plate
- surfaces of p-pad wire plate
- bottom substrate surface (in chip configurations with a substrate)

The user should also specify the initial die temperature. If *Isothermal Current Spreading* is solved, this temperature is considered as the device operating temperature at which the current spreading is simulated.

4.9 Computation Run

The computational module is invoked in a separate window named **SpeCLED Solver** providing brief information on the solution process, such as the type of the problem, time of

the start of the problem and completion of the computation. This window includes a panel which provides pictorial visualization of the iterative solution process.

The current spreading computation can be carried out either for a single value of total current or for a range of the current variation.

In case of computation for a single value of total current specified by the user, the simulation of coupled heat transfer and current spreading is organized as a series of global iterations of current spreading at a fixed temperature distribution and heat transfer at a given current flow as follows:

1. Initial constant temperature is assigned.
2. Current spreading at a given temperature distribution, with the total current as an input parameter. This problem, in turn, is organized as a series of iterations of the current spreading with the forward bias as an input parameter. The bias is varied to fit the required value of total current.
3. After current distribution providing the specified total current at a given temperature distribution is found, the heat transfer problem is solved.
4. Return to step 2, calculating the current spreading at a new temperature distribution.

The computations at each global iteration stop automatically as soon as the convergence is reached (i.e. the residuals become smaller than a given value and relative variation of the total current and maximum temperature becomes smaller than a given value) or the maximum number of iterations has been performed. The whole computation is stopped if the relative variation of the total current and maximum temperature during a single global iteration becomes smaller than a given value. The user can save intermediate results or to terminate the process manually. The results obtained are stored into files to be viewed using **SimuLEDView**.

In case of computation for a wide range of total current, the simulation of coupled heat transfer and current spreading is organized as follows:

- Computation for the value of current at the low edge of the specified range is made as described above. The forward bias corresponding to this value of current is stored.

- Consecutive computation for increasing values of the forward biases until the found total current exceeds the high edge of the specified range. The step of the bias variation is assigned by the user.

4.10 Visualization of the Computation Results

The results of the computation are stored in ASCII files (*.cgs) viewed by a specialized visualization tool **SimuLEDView** supplied with **SpeCLED & RATRO**. It provides visualization of various distributions over the active region and in various horizontal 2D cross sections of the die bulk, and integral parameters including the total current and wall plug efficiency. If several files with the same chip at different currents are loaded, the integral characteristics can be plotted as functions of current.

5 Getting Started with RATRO

SpeCLED and **RATRO** share the same geometry data, so specification of the chip geometry is done in **RATRO** in the same way as in **SpeCLED**, as discussed in Sections 4.2, 4.3, and 4.4. Below, we will describe actions specific for **RATRO** simulations.

5.1 Optical Properties of Bulk Blocks

The user has to assign the following properties of n- and p-semiconductor layers, substrate and immersion medium:

- Refraction index. It can be specified constant or dependent of wavelength using the first-order Sellmeier approximation $n^2(\lambda) = 1 + a_1 \frac{\lambda^2}{\lambda^2 - b_1^2}$
- Absorption index, cm^{-1}. It can be specified constant or dependent of wavelength and donor concentration using the following approximation: $\alpha(\lambda) = \alpha_0 + A\lambda^2 n$. Here, ***n*** is the major carrier concentration.

RATRO includes a set of predefined bulk semiconductor materials including n- and p-GaN, GaAs, AlN, sapphire, 4H- and 6H-SiC, and several epoxy grades.

5.2 Optical Properties of Internal and External Interfaces

In addition to specification of the bulk material characteristics, the user should assign the optical properties for each internal and external interface, like free surfaces of n- and p-semiconductor layers, surfaces covered by electrodes and pads, the interface between the substrate and the heterostructure, etc.

The following surface models are supported

- Smooth Surface. This type can be assigned to all metal-free surfaces, i.e. the n- and p-semiconductor layer free surfaces, substrate or n-semiconductor layer bottom surfaces and heterostructure/substrate interface. Besides, this type is automatically assigned to all lateral chip surfaces. For a smooth surface, the reflection and transmission coefficients are calculated for TE and TM polarized waves according to the Fresnel's relationships.
- Mirror. This type can be assigned for any surface. For a Mirror surface, the reflection and refraction angles correspond to the case of a smooth surface, but the reflection (R) and transmission (T) coefficients are assigned by the user, while the absorption coefficient (A) is found as A = 1 – R – T. The assigned values are used unless the incidence angle exceeds the total internal reflection angle. In case of total internal reflection T = 0, R = 1 – A, while A is assumed to be constant in the whole angle range.
- Full Absorption. A type that can be assigned to n- and p-pads. It corresponds to the Mirror surface with A = 1.
- Multiple Layer. This type can be assigned for any surface. A multiple layer can consist of one or several layers of different materials and thickness. The effective reflection, absorption and transmission coefficients of such surface are calculated by the program accounting for the interference in the multilayer contact. The user should specify the number of layers, material and thickness of each layer.
- Hexagonal Facets, Rectangular Facets, and Hemisphere Facets. These types can be assigned to all metal-free surfaces, i.e. the n- and p-semiconductor layer free surfaces, substrate or n-semiconductor layer bottom surfaces and heterostructure/substrate interface. They represent regularly patterned surfaces with hexagonal and rectangular facets, respectively. The user should assign the geometric parameters of each facet.

- Multiple Layer on Facets. This type is combination of 'Multiple Layer' and 'Facets' options to described a patterned surfaces covered with some layer refractive layer (say, metal electrode on top of the facetted semiconductor or ITO layer). The ray tracing is done in a way described for the facets of the same geometry, while probabilities of the ray refraction, transmission, and absorption are computed from the multiple layer model.

5.3 Heterostructure Emission Parameters

In addition to specification of the bulk and surface properties, the user has to assign the following parameters of the light emission:

- Wavelength of the emission that affects all wavelength-dependent parameters.
- Light polarization. **RATRO** can trace both polarized and non polarized light. If polarization is enabled by the user, TE and TM rays are traced independently. For polarized light, the user assigns the initial emission polarization, the probability of emission of TE or TM ray. If polarization is disabled, the reflection and transmission coefficients of each ray are calculated as an average value of the TE and TM polarizations.
- Lateral Intensity Distribution. Two options are available:
  - ✓ Distribution of the intensity of emission from the active region can be imported from a file generated by **SpeCLED** as a result of solving the current spreading problem. Note that the emission wavelength distribution calculated by **SpeCLED** is ignored, and the constant emission wavelength assign by the user is always used.
  - ✓ As an alternative, a uniform distribution of the intensity of emission from the active region is assigned. If **RATRO** is used without **SpeCLED**, this is the only mode available.
- Angular Emission Distribution. Specification of the angular distribution of the emission from the active region. Three options are supported and the resulting distribution is shown in the plot:
  - ❖ *Isotropic*. The active region is assumed to emit isotropic light, i.e. power emitted into a unit space angle does not depend on the ray direction (recommended choice).

❖ *Lambert's Law*. The active region is assumed to emit as a lambertian surface. The power emitted into a unit space angle depends on the polar angle θ as $I(\theta) \sim I_0 \cos\theta$.

❖ *Table*. This option allows input of custom angular distribution. The distribution can be loaded from a text file using the *Load* button. The file should contain two columns of values separated by tab. First column is for the angle in degrees, second is for the probability. Zero angle refers to the normal direction in top direction (from n-side to p-side).